Spartan-3E FPGA Family: Complete Data Sheet

DS312 May 19, 2006

Preliminary Product Specification

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DS312-1 (v3.0) March 22, 2006

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Spartan-3E FPGA Family: Introduction and Ordering Information

DS312-1 (v3.0) March 22, 2006

Preliminary Product Specification

Introduction

The Spartan™-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates, as shown in Table 1.

The Spartan-3E family builds on the success of the earlier Spartan-3 family by increasing the amount of logic per I/O, significantly reducing the cost per logic cell. New features improve system performance and reduce the cost of configuration. These Spartan-3E enhancements, combined with advanced 90 nm process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3E FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3E family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Features

- Very low cost, high-performance logic solution for high-volume, consumer-oriented applications
- Proven advanced 90-nanometer process technology
- Multi-voltage, multi-standard SelectIO™ interface pins
    - Up to 376 I/O pins or 156 differential signal pairs
    - LVCMOS, LVTTL, HSTL, and SSTL single-ended signal standards
    - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
    - 622+ Mb/s data transfer rate per I/O
    - True LVDS, RSDS, mini-LVDS, differential HSTL/SSTL differential I/O
    - Enhanced Double Data Rate (DDR) support
    - DDR SDRAM support up to 333 Mb/s
- Abundant, flexible logic resources
    - Densities up to 33,192 logic cells, including optional shift register or distributed RAM support
    - Efficient wide multiplexers, wide logic
    - Fast look-ahead carry logic
    - Enhanced 18 x 18 multipliers with optional pipeline
    - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
    - Up to 648 Kbits of fast block RAM
    - Up to 231 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
    - Clock skew elimination (delay locked loop)
    - Frequency synthesis, multiplication, division
    - High-resolution phase shifting
    - Wide frequency range (5 MHz to over 300 MHz)
- Eight global clocks plus eight additional clocks per each half of device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
    - Low-cost, space-saving SPI serial Flash PROM
    - x8 or x8/x16 parallel NOR Flash PROM
    - Low-cost Xilinx Platform Flash with JTAG
- Complete Xilinx ISE™ and WebPACK™ development system support
- MicroBlaze™ and PicoBlaze™ embedded processor cores
- Fully compliant 32-/64-bit 33 MHz PCI support
- Low-cost QFP and BGA packaging options
    - Common footprints support easy density migration
    - Pb-free packaging options

Table 1: **Summary of Spartan-3E FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits[1]	Block RAM bits[1]	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232	92
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

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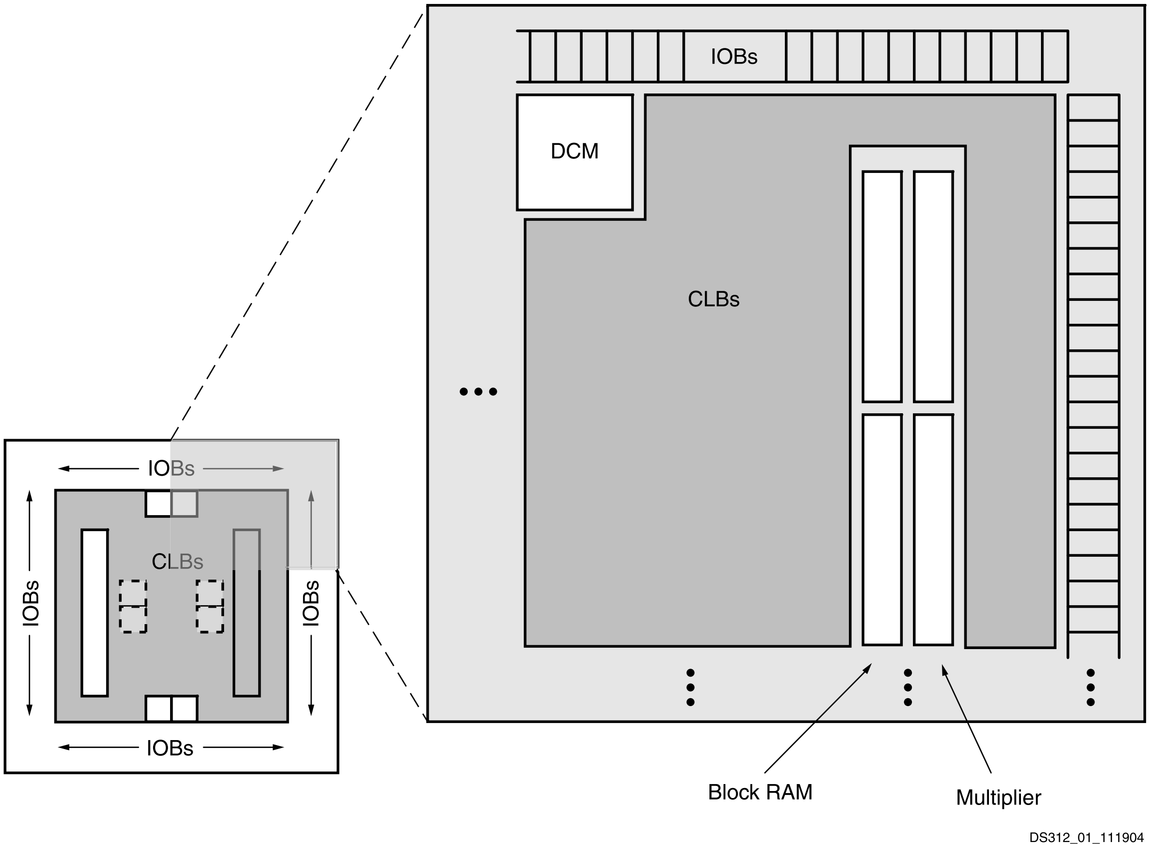
Architectural Overview

The Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S100E has only one DCM at the top and bottom, while the XC3S1200E and XC3S1600E add two DCMs in the middle of the left and right sides.

The Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3S1200E and XC3S1600E have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S100E has only one DCM at the top and one at the bottom.

Figure 1: **Spartan-3E Family Architecture**

Configuration

Spartan-3E FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up or Down from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester.

I/O Capabilities

The Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Spartan-3E FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Device	VQ100 VQG100		CP132 CPG132		TQ144 TQG144		PQ208 PQG208		FT256 FTG256		FG320 FGG320		FG400 FGG400		FG484 FGG484	
	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S100E	**66** *(7)*	**30** *(2)*	**83** *(11)*	**35** *(2)*	**108** *(28)*	**40** *(4)*	-	-	-	-	-	-	-	-	-	-
XC3S250E	**66** *(7)*	**30** *(2)*	**92** *(7)*	**41** *(2)*	**108** *(28)*	**40** *(4)*	**158** *(32)*	**65** *(5)*	**172** *(40)*	**68** *(8)*	-	-	-	-	-	-
XC3S500E	-	-	**92** *(7)*	**41** *(2)*	-	-	**158** *(32)*	**65** *(5)*	**190** *(41)*	**77** *(8)*	**232** *(56)*	**92** *(12)*	-	-	-	-
XC3S1200E	-	-	-	-	-	-	-	-	**190** *(40)*	**77** *(8)*	**250** *(56)*	**99** *(12)*	**304** *(72)*	**124** *(20)*	-	-
XC3S1600E	-	-	-	-	-	-	-	-	-	-	**250** *(56)*	**99** *(12)*	**304** *(72)*	**124** *(20)*	**376** *(82)*	**156** *(21)*

Notes:

1. All Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4: **Pinout Descriptions**.
2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins.

Package Marking

Figure 2 provides a top marking example for Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3E FPGAs in the CP132 and CPG132 packages.

Use the seven digits of the Lot Code to access additional information for a specific device using the Xilinx web-based Genealogy Viewer.

On the QFP and BGA packages, the optional numerical Stepping Code follows the Lot Code. If no Stepping Code appears, then the device is Stepping 0.

The “`5C`” and “`4I`” part combinations may be dual marked as “`5C/4I`”. All “`5C`” and “`4I`” part combinations use the Stepping 1 production silicon and have a ‘1’ Stepping Code mark.

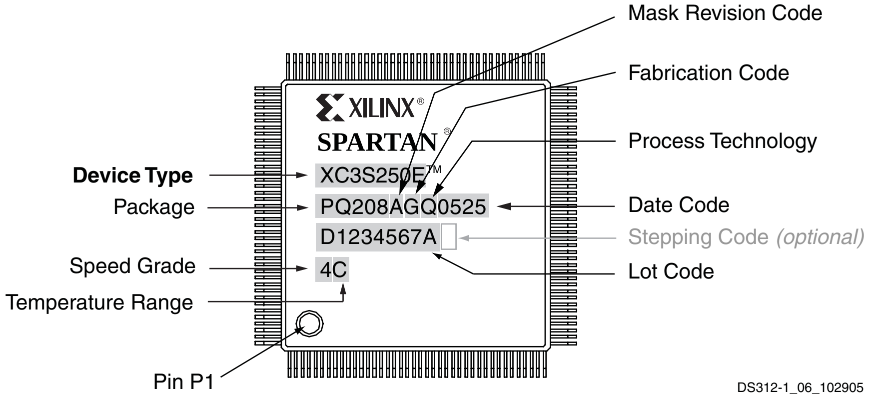


Figure 2: **Spartan-3E QFP Package Marking Example**

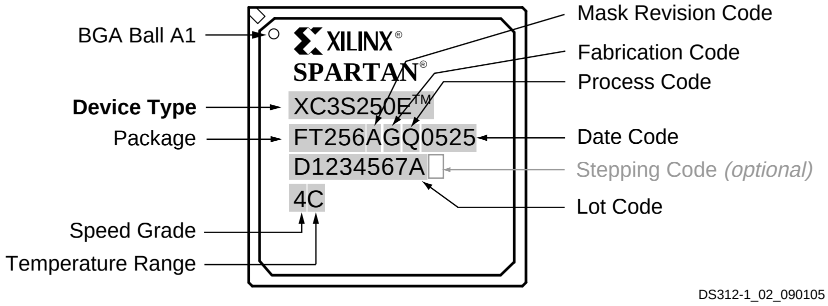


Figure 3: **Spartan-3E BGA Package Marking Example**

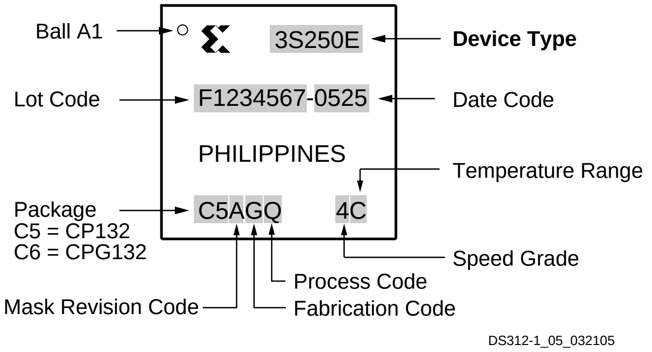
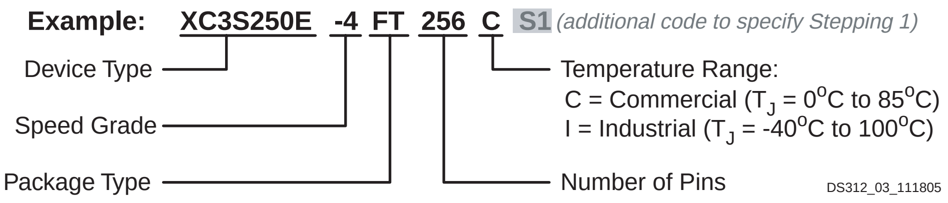


Figure 4: **Spartan-3E CP132 and CPG132 Package Marking Example**

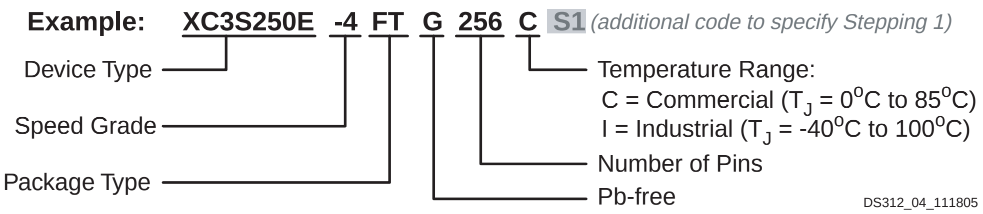
Ordering Information

Spartan-3E FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. All devices are available in Pb-free packages, which adds a ‘G’ character to the ordering code. All devices are available in either Commercial (C) or Industrial (I) temperature ranges. Both the standard –4 and faster –5 speed grades are available for the Commercial temperature range. However, only the –4 speed grade is available for the Industrial temperature range. See Table 2 for valid device/package combinations.

Standard Packaging



Pb-Free Packaging



Device
XC3S100E
XC3S250E
XC3S500E
XC3S1200E
XC3S1600E

Speed Grade	
–4	Standard Performance
–5	High Performance

Package Type / Number of Pins	
VQ(G)100	100-pin Very Thin Quad Flat Pack (VQFP)
CP(G)132	132-ball Chip-Scale Package (CSP)
TQ(G)144	144-pin Thin Quad Flat Pack (TQFP)
PQ(G)208	208-pin Plastic Quad Flat Pack (PQFP)
FT(G)256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)
FG(G)320	320-ball Fine-Pitch Ball Grid Array (FBGA)
FG(G)400	400-ball Fine-Pitch Ball Grid Array (FBGA)
FG(G)484	484-ball Fine-Pitch Ball Grid Array (FBGA)

Temperature Range (T_J)	
C	Commercial (0°C to 85°C)
I	Industrial (–40°C to 100°C)

Notes:

1. The –5 speed grade is exclusively available in the Commercial temperature range.

Production Stepping

The Spartan-3E FPGA family uses production stepping to indicate improved capabilities or enhanced features.

All devices ordered using the standard part number support Stepping 0 functionality and performance. Later steppings are, by definition, a functional superset of any previous stepping. Furthermore, configuration bitstreams generated for any stepping are forward compatible. See Table 71 for additional details.

When a new stepping is released to production, Xilinx will ship either the previous or new stepping version for a time before shipping only the new version. Designs operating on the current stepping perform similarly on a later stepping level.

To specify only the later stepping, append an *S#* suffix to the standard ordering code, where *#* is the stepping number, as indicated in Table 3.

Table 3: **Spartan-3E Stepping Levels**

Stepping Number	Suffix Code	Status
0	None or S0	Production
1	S1	Planned

Beginning with Stepping 1 and later, the stepping level is marked on the device using a single number character, as shown in Figure 2, Figure 3, and Figure 4. Stepping 0 devices are represented with either a '0' mark or no mark.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in CP132 package to Table 2. Corrected number of differential I/O pairs for CP132 package. Added package markings for QFP packages (Figure 2) and CP132/CPG132 packages (Figure 4).
11/23/05	2.0	Added differential HSTL and SSTL I/O standards. Updated Table 2 to indicate number of input-only pins. Added **Production Stepping** information, including example top marking diagrams.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Added XC3S100E in CP132 package and updated I/O counts for the XC3S1600E in FG320 package (Table 2). Added information about dual markings for –5C and –4I product combinations to **Package Marking**.

Spartan-3E FPGA Family: Functional Description

DS312-2 (v3.2) May 19, 2006

Preliminary Product Specification

Introduction

As described in **Architectural Overview**, the Spartan™-3E FPGA architecture consists of five fundamental functional elements:

- **Input/Output Blocks (IOBs)**
- **Configurable Logic Block (CLB) and Slice Resources**
- **Block RAM**
- **Dedicated Multipliers**
- **Digital Clock Managers (DCMs)**

The following sections provide detailed information on each of these functions. In addition, this section also describes the following functions:

- **Clocking Infrastructure**
- **Interconnect**
- **Configuration**
- **Powering Spartan-3E FPGAs**

Input/Output Blocks (IOBs)

IOB Overview

The Input/Output Block (IOB) provides a programmable, unidirectional or bidirectional interface between a package pin and the FPGA's internal logic. The IOB is similar to that of the Spartan-3 family with the following differences:

- Input-only blocks are added
- Programmable input delays are added to all blocks
- DDR flip-flops can be shared between adjacent IOBs

The unidirectional input-only block has a subset of the full IOB capabilities. Thus there are no connections or logic for an output path. The following paragraphs assume that any reference to output functionality does not apply to the input-only blocks. The number of input-only blocks varies with device size, but is never more than 25% of the total IOB count.

Figure 5, page 10 is a simplified diagram of the IOB's internal structure. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see **Storage Element Functions**. The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. After the delay element, there are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 lead to the FPGA's internal logic. The delay element can be set to ensure a hold time of zero (see **Input Delay Functions**).
- The output path, starting with the O1 and O2 lines, carries data from the FPGA's internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA's internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

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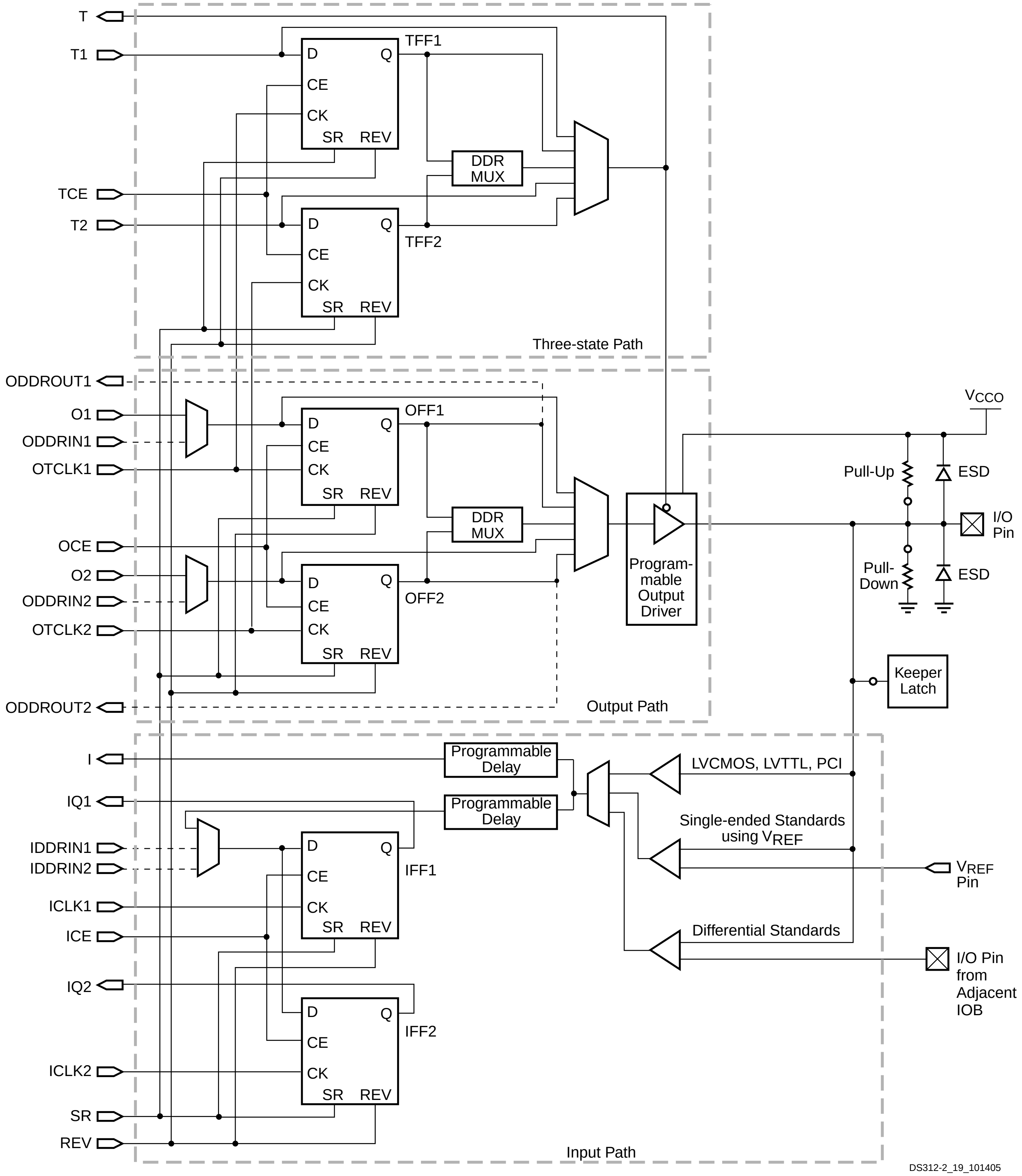

Notes:

1. All IOB control and output path signals have an inverting polarity option wihtin the IOB.
2. Signals shown with dashed lines connect to the adjacent IOB in a differential pair only, not to the FPGA fabric.

Figure 5: **Simplified IOB Diagram**

Input Delay Functions

Each IOB has a programmable delay block that can delay the input signal from 0 to nominally 6000 ps. In Figure 6, the signal is first delayed by either 0 or 4000 ps (nominal) and is then applied to a 7-tap delay line. This delay line has a nominal value of 250 ps per tap. All seven taps are available via a multiplexer for use as an asynchronous input directly into the FPGA fabric. In this way, the delay is programmable from 0 to 6000 ps in ~250 ps steps. Three of the seven taps are also available via a multiplexer to the D inputs of the synchronous storage elements. The delay inserted in the path to the storage element can be varied from 0 to 6000 ps in 500 ps steps. The first, coarse delay element is common to both asynchronous and synchronous paths, and must be either used or not used for both paths.

The delay values are set up in the silicon once at configuration time—they are non-modifiable in device operation.

The primary use for the input delay element is as an adequate delay to ensure that there is no hold time requirement when using the input flip-flop(s) with a global clock. The necessary value for this function is chosen by the Xilinx software tools and depends on device size. If the design is using a DCM in the clock path, then the delay element can be safely set to zero in the user's design, and there is still no hold time requirement.

Both asynchronous and synchronous values can be modified by the user, which is useful where extra delay is required on clock or data inputs, for example, in interfaces to various types of RAM.

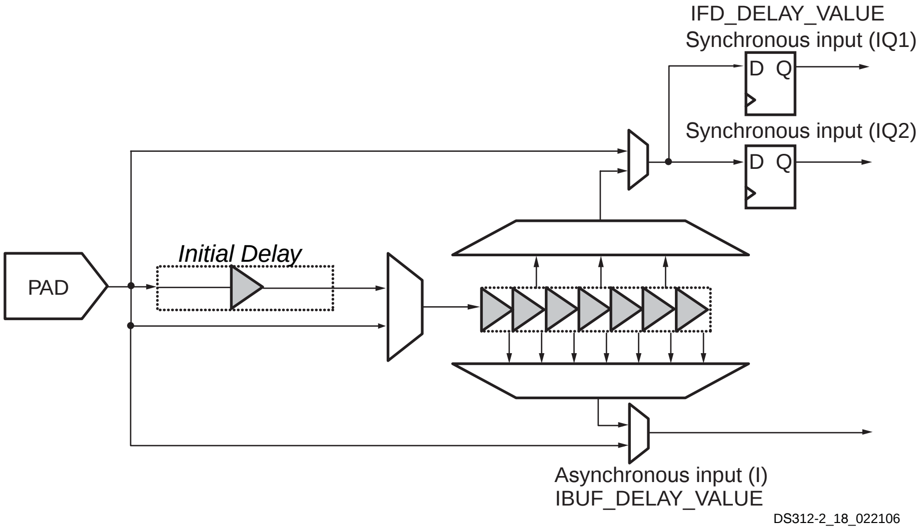

Figure 6: **Programmable Fixed Input Delay Elements**

Storage Element Functions

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

The storage-element pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal's rising edge and converting it to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (ODDR2).

Table 4 describes the signal paths associated with the storage element.

Table 4: **Storage Element Signal Description**

Storage Element Signal	Description	Function
D	Data input	Data at this input is stored on the active edge of CK and enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q.
Q	Data output	The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q mirrors the data at D.
CK	Clock input	Data is loaded into the storage element on this input's active edge with CE asserted.
CE	Clock Enable input	When asserted, this input enables CK. If not connected, CE defaults to the asserted state.
SR	Set/Reset input	This input forces the storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0.
REV	Reverse input	This input is used together with SR. It forces the storage element into the state opposite from what SR does. The SYNC/ASYNC attribute setting determines whether the REV input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0.

As shown in Figure 5, the upper registers in both the output and three-state paths share a common clock. The OTCLK1 clock signal drives the CK clock inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 drives the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2.

The OCE enable line controls the CE inputs of the upper and lower registers on the output path. Similarly, TCE controls the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path.

The Set/Reset (SR) line entering the IOB controls all six registers, as is the Reverse (REV) line.

In addition to the signal polarity controls described in **IOB Overview**, each storage element additionally supports the controls described in Table 5.

Table 5: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-triggered flip-flop or a level-sensitive latch	Independent for each storage element
SYNC/ASYNC	Determines whether the SR set/reset control is synchronous or asynchronous	Independent for each storage element

Table 5: **Storage Element Options *(Continued)***

Option Switch	Function	Specificity
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic "1" (SRHIGH) or a Reset, which forces a logic "0" (SRLOW)	Independent for each storage element, except when using ODDR2. In the latter case, the selection for the upper element will apply to both elements.
INIT1/INIT0	When Global Set/Reset (GSR) is asserted or after configuration this option specifies the initial state of the storage element, either set (INIT1) or reset (INIT0). By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using ODDR2, which uses two IOBs. In the ODDR2 case, selecting INIT0 for one IOBs applies to both elements within the IOB, although INIT1 could be selected for the elements in the other IOB.

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3E devices use register pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB's Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (ODDR2). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. DDR operation requires two clock signals (usually 50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 7. The Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, and then shifting it 180 degrees. This approach ensures minimal skew between the two signals. Alternatively, the inverter inside the IOB can be used to invert the clock signal, thus only using one clock line and both rising and falling edges of that clock line as the two clocks for the DDR flip-flops.

The storage-element pair on the Three-State path (TFF1 and TFF2) also can be combined with a local multiplexer to form a DDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register, and the inverted clock signal triggers the other register. The registers take turns capturing bits of the incoming DDR data signal. The primitive to allow this functionality is called IDDR2.

Aside from high bandwidth data transfers, DDR outputs also can be used to reproduce, or *mirror*, a clock signal on the output. This approach is used to transmit clock and data signals together (source synchronously). A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs is minimal.

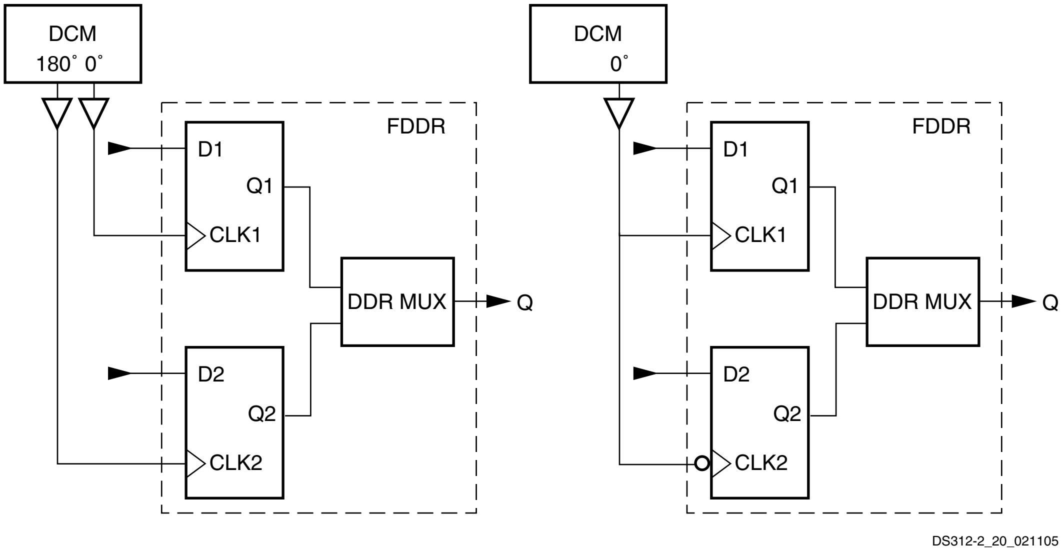

Figure 7: **Two Methods for Clocking the DDR Register**

Register Cascade Feature

In the Spartan-3E family, one of the IOBs in a differential pair can cascade either its input or output storage elements with those in the other IOB of the differential pair. This is intended to make DDR operation at high speed much simpler to implement. The new DDR connections that are available are shown in Figure 5 (dashed lines), and are only available for routing between IOBs and are not accessible to the FPGA fabric. Note that this feature is only available when using differential I/O.

IDDR2

As a DDR input pair, the master IOB registers incoming data on the rising edge of ICLK1 (= D1) and the rising edge of ICLK2 (= D2), which is typically the same as the falling edge of ICLK1. This data is then transferred into the FPGA fabric. At some point, both signals must be brought into the same clock domain, typically ICLK1. This can be difficult at high frequencies because the available time is only one half of a clock cycle assuming a 50% duty cycle. See Figure 8 for a graphical illustration of this function.

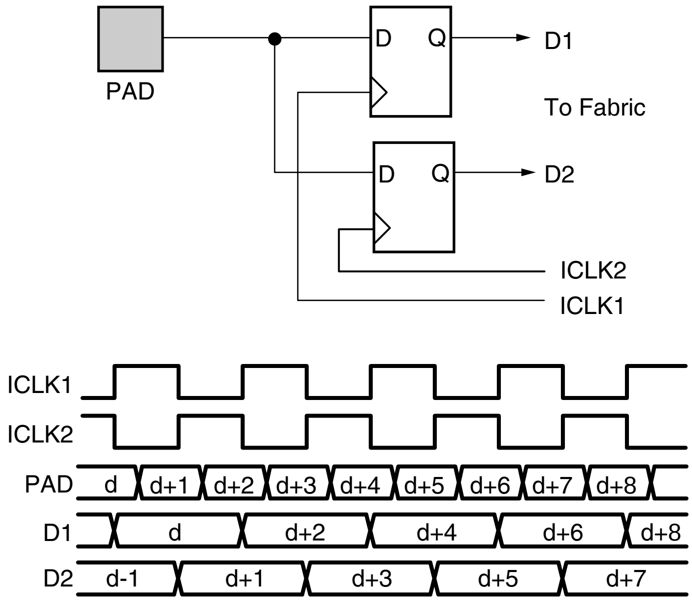

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Figure 8: **Input DDR (without Cascade Feature)**

In the Spartan-3E device, the signal D2 can be cascaded into the storage element of the adjacent slave IOB. There it is re-registered to ICLK1, and only then fed to the FPGA fabric where it is now already in the same time domain as D1. Here, the FPGA fabric uses only the clock ICLK1 to process the received data. See Figure 9 for a graphical illustration of this function.

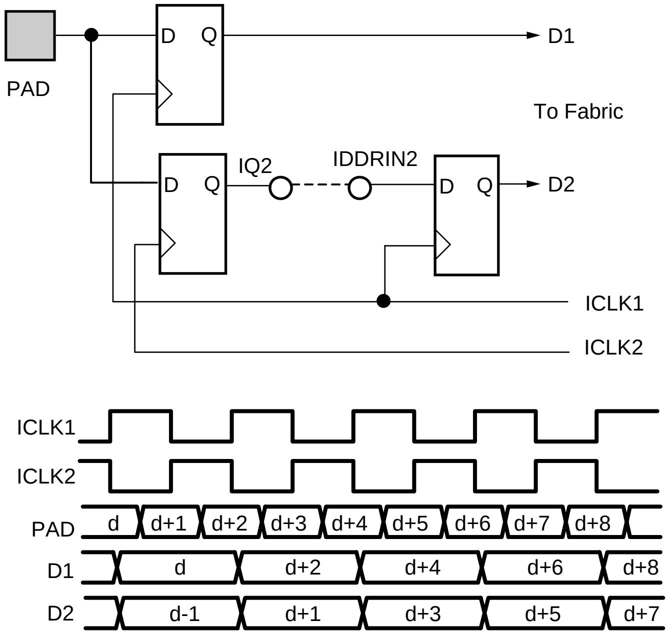

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Figure 9: **Input DDR Using Spartan-3E Cascade Feature**

ODDR2

As a DDR output pair, the master IOB registers data coming from the FPGA fabric on the rising edge of OCLK1 (= D1) and the rising edge of OCLK2 (= D2), which is typically the same as the falling edge of OCLK1. These two bits of data are multiplexed by the DDR mux and forwarded to the output pin. At some point in the FPGA fabric, the signal D2 must be brought into the clock domain OCLK2 from the domain OCLK1. This can be difficult at high frequencies, because the time available is only one half a clock cycle. See Figure 10 for a graphical illustration of this function.

In the Spartan-3E device, the signal D2 can be cascaded via the storage element of the adjacent slave IOB. Here, it is registered by OCLK1 and then forwarded to the master IOB where it is re-registered to OCLK2, selected as usual by the DDR multiplexer, and then forwarded to the output pin. This way the data for transmission can be processed using just the clock OCLK1 in the FPGA fabric. See Figure 11 for a graphical illustration of this function.

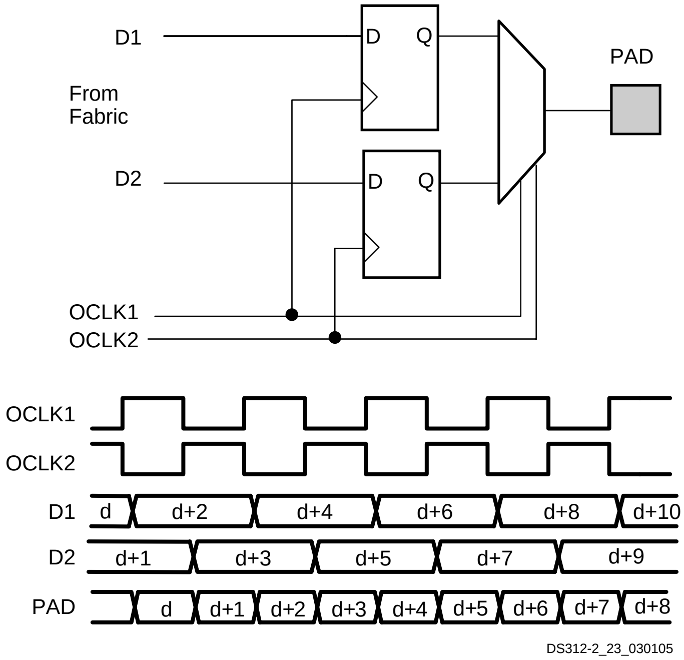

Figure 10: **Output DDR (without Cascade Feature)**

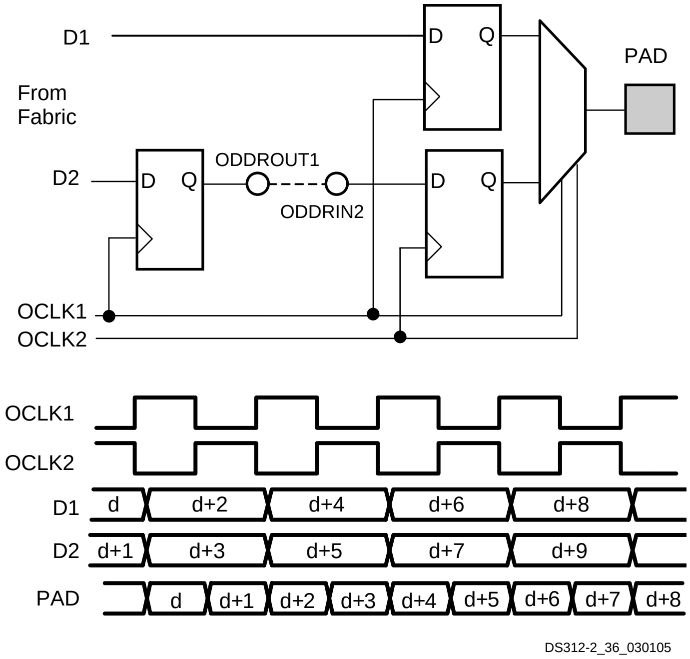

Figure 11: **Output DDR Using Spartan-3E Cascade Feature**

SelectIO Signal Standards

The Spartan-3E I/Os feature inputs and outputs that support a wide range of I/O signaling standards (Table 6 and Table 7). The majority of the I/Os also can be used to form differential pairs to support any of the differential signaling standards (Table 7).

To define the I/O signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to “Entry Strategies for Xilinx Constraints” in the Xilinx Software Manuals and Help.

Spartan-3E FPGAs provide additional input flexibility by allowing I/O standards to be mixed in different banks. Special care must be taken to ensure the input voltages do not exceed V_{CCO} (see **DC and Switching Characteristics** in Module 3 for the specifications). For a particular V_{CCO} voltage, Table 6 and Table 7 list all of the IOSTANDARDs that can be combined and if the IOSTANDARD is supported as an input only or can be used for both inputs and outputs.

Table 6: **Single-Ended IOSTANDARD Bank Compatibility**

Single-Ended IOSTANDARD	V_{CCO} Supply/Compatibility						Input Requirements	
	1.2V	1.5V	1.8V	2.5V	3.0V	3.3V	V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	-	-	-	-	-	Input/ Output	N/R(1)	N/R
LVCMOS33	-	-	-	-	-	Input/ Output	N/R	N/R
LVCMOS25	-	-	-	Input/ Output	Input	Input	N/R	N/R
LVCMOS18	-	-	Input/ Output	Input	Input	Input	N/R	N/R
LVCMOS15	-	Input/ Output	Input	Input	Input	Input	N/R	N/R
LVCMOS12	Input/ Output	Input	Input	Input	Input	Input	N/R(1)	N/R
PCI33_3	-	-	-	-	Input/ Output(2)	Input(3)	N/R	N/R
PCI66_3	-	-	-	-	Input/ Output(2)	Input(3)	N/R	N/R
PCIX					Input/ Output(2)	Input(3)	N/R	N/R
HSTL_I_18	-	-	Input/ Output	Input	Input	Input	0.9	0.9
HSTL_III_18	-	-	Input/ Output	Input	Input	Input	1.1	1.8
SSTL18_I	-	-	Input/ Output	Input	Input	Input	0.9	0.9
SSTL2_I	-	-	-	Input/ Output	Input	Input	1.25	1.25

Notes:

1. N/R - Not required for input operation.
2. Fully-compliant PCI plug-in applications require V_{CCO} = 3.0V as described in XAPP653: *Virtex™-II Pro and Spartan-3 3.3V PCI Reference Design*. Also see Note 3.
3. Point-to-point or chip-to-chip PCI interfaces, such as those that connect the FPGA to a processor or ASP via a PCI on a single printed circuit board, may optionally use a 3.3V V_{CCO}.

Table 7: **Differential IOSTANDARD Bank Compatibility**

Differential IOSTANDARD	**V_{CCO} Supply**			**Input Requirements: V_{REF}**	**Differential Bank Restriction(1)**
	1.8V	**2.5V**	**3.3V**		
LVDS_25	Input	Input, On-chip Differential Termination, Output	Input	V_{REF} is not used for these I/O standards	Applies to Outputs Only
RSDS_25	Input	Input, On-chip Differential Termination, Output	Input		Applies to Outputs Only
MINI_LVDS_25	Input	Input, On-chip Differential Termination, Output	Input		Applies to Outputs Only
LVPECL_25	Input	Input	Input		No Differential Bank Restriction (other I/O bank restrictions might apply)
BLVDS_25	Input	Input, Output	Input		
DIFF_HSTL_I_18	Input, Output	Input	Input		
DIFF_HSTL_III_18	Input, Output	Input	Input		
DIFF_SSTL18_I	Input, Output	Input	Input		
DIFF_SSTL2_I	Input	Input, Output	Input		

Notes:

1. Each bank can support any two of the following: LVDS_25 outputs, MINI_LVDS_25 outputs, RSDS_25 outputs.

HSTL and SSTL inputs use the Reference Voltage (V_{REF}) to bias the input-switching threshold. Once a configuration data file is loaded into the FPGA that calls for the I/Os of a given bank to use HSTL/SSTL, a few specifically reserved I/O pins on the same bank automatically convert to V_{REF} inputs. For banks that do not contain HSTL or SSTL, V_{REF} pins remain available for user I/Os or input pins.

Differential standards employ a pair of signals, one the opposite polarity of the other. The noise canceling properties (for example, Common-Mode Rejection) of these standards permit exceptionally high data transfer rates. This subsection introduces the differential signaling capabilities of Spartan-3E devices.

Each device-package combination designates specific I/O pairs specially optimized to support differential standards. Differential pairs can be shown in the Pin and Area Constraints Editor (PACE) with the “Show Differential Pairs” option. A unique *L-number*, part of the pin name, identifies the line-pairs associated with each bank (see **Pinout Descriptions** in Module 4). For each pair, the letters *P* and *N* designate the true and inverted lines, respectively. For example, the pin names IO_L43P_3 and IO_L43N_3 indicate the true and inverted lines comprising the line pair L43 on Bank 3.

V_{CCO} provides current to the outputs and additionally powers the On-Chip Differential Termination. V_{CCO} must be 2.5V when using the On-Chip Differential Termination. The V_{REF} lines are not required for differential operation.

To further understand how to combine multiple IOSTANDARDs within a bank, refer to **IOBs Organized into Banks**, page 19.

On-Chip Differential Termination

Spartan-3E devices provide an on-chip ~120Ω differential termination across the input differential receiver terminals. The on-chip input differential termination in Spartan-3E devices potentially eliminates the external 100Ω termination resistor commonly found in differential receiver circuits. Differential termination is used for LVDS, mini-LVDS, and RSDS as applications permit.

On-chip Differential Termination is available in banks with V_{CCO} = 2.5V and is not supported on dedicated input pins. Set the DIFF_TERM attribute to TRUE to enable Differential Termination on a differential I/O pin pair.

The DIFF_TERM attribute uses the following syntax in the UCF file:

```
INST <I/O_BUFFER_INSTANTIATION_NAME>
DIFF_TERM = “<TRUE/FALSE>”;
```

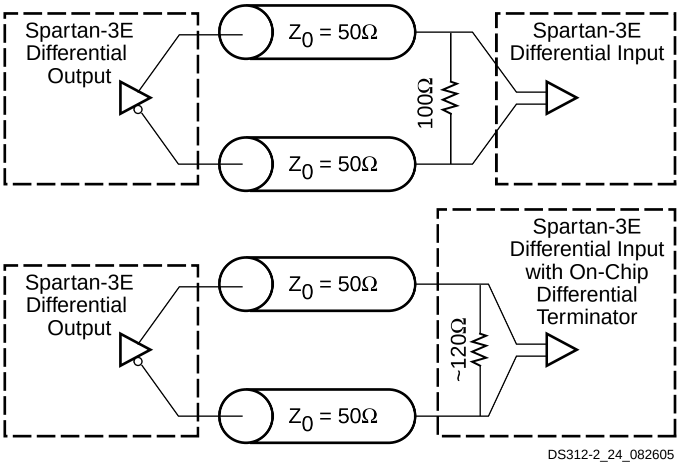

Figure 12: **Differential Inputs and Outputs**

Pull-Up and Pull-Down Resistors

Pull-up and pull-down resistors inside each IOB optionally force a floating I/O or Input-only pin to a determined state. Pull-up and pull-down resistors are commonly applied to unused I/Os, inputs, and three-state outputs, but can be used on any I/O or Input-only pin. The pull-up resistor connects an IOB to V_{CCO} through a resistor. The resistance value depends on the V_{CCO} voltage (see **DC and Switching Characteristics** in Module 3 for the specifications). The pull-down resistor similarly connects an IOB to ground with a resistor. The PULLUP and PULLDOWN attributes and library primitives turn on these optional resistors.

By default, PULLDOWN resistors terminate all unused I/O and Input-only pins. Unused I/O and Input-only pins can alternatively be set to PULLUP or FLOAT. To change the unused I/O Pad setting, set the Bitstream Generator (BitGen) option ***UnusedPin*** to PULLUP, PULLDOWN, or FLOAT. The ***UnusedPin*** option is accessed through the Properties for Generate Programming File in ISE. See **Bitstream Generator (BitGen) Options**.

During configuration a Low logic level on the HSWAP pin activates pull-up resistors on all I/O and Input-only pins not actively used in the selected configuration mode.

Keeper Circuit

Each I/O has an optional keeper circuit (see Figure 13) that keeps bus lines from floating when not being actively driven. The KEEPER circuit retains the last logic level on a line after all drivers have been turned off. Apply the KEEPER attribute or use the KEEPER library primitive to use the KEEPER circuitry. Pull-up and pull-down resistors override the KEEPER settings.

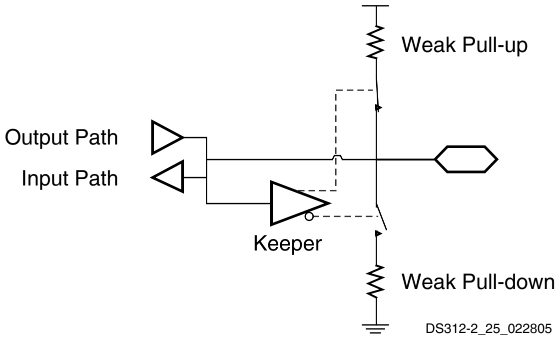

Figure 13: **Keeper Circuit**

Slew Rate Control and Drive Strength

Each IOB has a slew-rate control that sets the output switching edge-rate for LVCMOS and LVTTL outputs. The SLEW attribute controls the slew rate and can either be set to SLOW (default) or FAST.

Each LVCMOS and LVTTL output additionally supports up to six different drive current strengths as shown in Table 8. To adjust the drive strength for each output, the DRIVE attribute is set to the desired drive strength: 2, 4, 6, 8, 12, and 16. Unless otherwise specified in the FPGA application, the software default IOSTANDARD is LVCMOS25, SLOW slew rate, and 12 mA output drive.

Table 8: **Programmable Output Drive Current**

IOSTANDARD	Output Drive Current (mA)					
	2	**4**	**6**	**8**	**12**	**16**
LVTTL	✓	✓	✓	✓	✓	✓
LVCMOS33	✓	✓	✓	✓	✓	✓
LVCMOS25	✓	✓	✓	✓	✓	-
LVCMOS18	✓	✓	✓	✓	-	-
LVCMOS15	✓	✓	✓	-	-	-
LVCMOS12	✓	-	-	-	-	-

High output current drive strength and FAST output slew rates generally result in fastest I/O performance. However, these same settings generally also result in transmission line effects on the printed circuit board (PCB) for all but the shortest board traces. Each IOB has independent slew rate and drive strength controls. Use the slowest slew rate and lowest output drive current that meets the performance requirements for the end application.

Likewise, due to lead inductance, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Only use fast, high-drive outputs when required by the application.

IOBs Organized into Banks

The Spartan-3E architecture organizes IOBs into four I/O banks as shown in Figure 14. Each bank maintains separate V_{CCO} and V_{REF} supplies. The separate supplies allow each bank to independently set V_{CCO}. Similarly, the V_{REF} supplies may be set for each bank. Refer to Table 6 and Table 7 for V_{CCO} and V_{REF} requirements.

When working with Spartan-3E devices, most of the differential I/O standards are compatible and can be combined within any given bank. Each bank can support any two of the following differential standards: LVDS_25 outputs, MINI_LVDS_25 outputs, and RSDS_25 outputs. As an example, LVDS_25 outputs, RSDS_25 outputs, and any other differential inputs while using on-chip differential termination are a valid combination. A combination not allowed is a single bank with LVDS_25 outputs, RSDS_25 outputs, and MINI_LVDS_25 outputs.

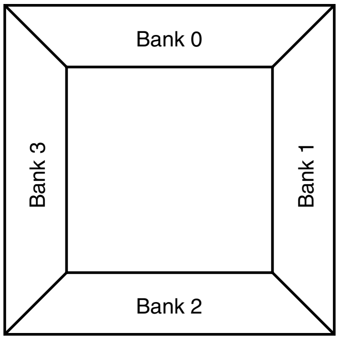

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Figure 14: **Spartan-3E I/O Banks (top view)**

I/O Banking Rules

When assigning I/Os to banks, these V_{CCO} rules must be followed:

1. All V_{CCO} pins on the FPGA must be connected even if a bank is unused.
2. All V_{CCO} lines associated within a bank must be set to the same voltage level.
3. The V_{CCO} levels used by all standards assigned to the I/Os of any given bank must agree. The Xilinx development software checks for this. Table 6 and Table 7 describe how different standards use the V_{CCO} supply.
4. If a bank does not have any V_{CCO} requirements, connect V_{CCO} to an available voltage, such as 2.5V or 3.3V. Some configuration modes might place additional V_{CCO} requirements. Refer to **Configuration** for more information.

If any of the standards assigned to the Inputs of the bank use V_{REF}, then the following additional rules must be observed:

1. All V_{REF} pins must be connected within a bank.
2. All V_{REF} lines associated with the bank must be set to the same voltage level.
3. The V_{REF} levels used by all standards assigned to the Inputs of the bank must agree. The Xilinx development software checks for this. Table 6 describes how different standards use the V_{REF} supply.

If V_{REF} is not required to bias the input switching thresholds, all associated V_{REF} pins within the bank can be used as user I/Os or input pins.

Package Footprint Compatibility

Sometimes, applications outgrow the logic capacity of a specific Spartan-3E FPGA. Fortunately, the Spartan-3E family is designed so that multiple part types are available in pin-compatible package footprints, as described in **Pinout Descriptions** in Module 4. In some cases, there are subtle differences between devices available in the same footprint. These differences are outlined for each package, such as pins that are unconnected on one device but connected on another in the same package or pins that are dedicated inputs on one package but full I/O on another. When designing the printed circuit board (PCB), plan for potential future upgrades and package migration.

The Spartan-3E family is not pin-compatible with any previous Xilinx FPGA family.

Dedicated Inputs

Dedicated Inputs are IOBs used only as inputs. Pin names designate a Dedicated Input if the name starts with *IP*, for example, IP or IP_Lxxx_x. Dedicated inputs retain the full functionality of the IOB for input functions with a single exception for differential inputs (IP_Lxxx_x). For the differential Dedicated Inputs, the on-chip differential termination is not available. To replace the on-chip differential termination, choose a differential pair that supports outputs (IO_Lxxx_x) or use an external 100Ω termination resistor on the board.

ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: one diode extends P-to-N from the pad to V_{CCO} and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3E I/Os to tolerate high signal voltages. The V_{IN} absolute maximum rating in Table 72 of **DC and Switching Characteristics** (Module 3) specifies the voltage range that I/Os can tolerate.

Supply Voltages for the IOBs

The IOBs are powered by three supplies:

1. The V_{CCO} supplies, one for each of the FPGA's I/O banks, power the output drivers. The voltage on the V_{CCO} pins determines the voltage swing of the output signal.
2. V_{CCINT} is the main power supply for the FPGA's internal logic.
3. V_{CCAUX} is an auxiliary source of power, primarily to optimize the performance of various FPGA functions such as I/O switching.

I/O and Input-Only Pin Behavior During Power-On, Configuration, and User Mode

In this section, all behavior described for I/O pins also applies to input-only pins and dual-purpose I/O pins that are not actively involved in the currently-selected configuration mode.

All I/O pins have ESD clamp diodes to their respective V_{CCO} supply and from GND, as shown in Figure 5. The V_{CCINT} (1.2V), V_{CCAUX} (2.5V), and V_{CCO} supplies can be applied in any order. Before the FPGA can start its configuration process, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} must have reached their respective minimum recommended operating levels indicated in Table 73. At this time, all output drivers are in a high-impedance state. V_{CCO} Bank 2, V_{CCINT}, and V_{CCAUX} serve as inputs to the internal Power-On Reset circuit (POR).

A Low level applied to the HSWAP input enables pull-up resistors on user-I/O and input-only pins from power-on throughout configuration. A High level on HSWAP disables the pull-up resistors, allowing the I/Os to float. HSWAP contains a weak pull-up and defaults to High if left floating. As soon as power is applied, the FPGA begins initializing its configuration memory. At the same time, the FPGA internally asserts the Global Set-Reset (GSR), which asynchronously resets all IOB storage elements to a default Low state. Also see **Pin Behavior During Configuration**.

Upon the completion of initialization and the beginning of configuration, INIT_B goes High, sampling the M0, M1, and M2 inputs to determine the configuration mode. Configuration data is then loaded into the FPGA. The I/O drivers remain in a high-impedance state (with or without pull-up resistors, as determined by the HSWAP input) throughout configuration.

At the end of configuration, the GSR net is released, placing the IOB registers in a Low state by default, unless the loaded design reverses the polarity of their respective SR inputs.

The Global Three State (GTS) net is released during Start-Up, marking the end of configuration and the beginning of design operation in the User mode. After the GTS net is released, all user I/Os go active while all unused I/Os are weakly pulled down (PULLDOWN). The designer can control how the unused I/Os are terminated after GTS is released by setting the Bitstream Generator (BitGen) option UnusedPin to PULLUP, PULLDOWN, or FLOAT.

One clock cycle later (default), the Global Write Enable (GWE) net is released allowing the RAM and registers to change states. Once in User mode, any pull-up resistors enabled by HSWAP revert to the user settings and HSWAP is available as a general-purpose I/O. For more information on PULLUP and PULLDOWN, see **Pull-Up and Pull-Down Resistors**.

Behavior of Unused I/O Pins After Configuration

By default, the Xilinx ISE development software automatically configures all unused I/O pins as input pins with individual internal pull-down resistors to GND.

This default behavior is controlled by the ***UnusedPin*** bitstream generator (BitGen) option, as described in Table 68.

JTAG Boundary-Scan Capability

All Spartan-3E IOBs support boundary-scan testing compatible with IEEE 1149.1/1532 standards. See **JTAG Mode** for more information on programming via JTAG.

Configurable Logic Block (CLB) and Slice Resources

CLB Overview

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB contains four slices, and each slice contains two Look-Up Tables (LUTs) to implement logic and two dedicated storage elements that can be used as flip-flops or latches. The LUTs can be used as a 16x1 memory (RAM16) or as a 16-bit shift register (SRL16), and additional multiplexers and carry logic simplify wide logic and arithmetic functions. Most general-purpose logic in a design is automatically mapped to the slice resources in the CLBs. Each CLB is identical, and the Spartan-3E family CLB structure is identical to that for the Spartan-3 family.

CLB Array

The CLBs are arranged in a regular array of rows and columns as shown in Figure 15.

Each density varies by the number of rows and columns of CLBs (see Table 9).

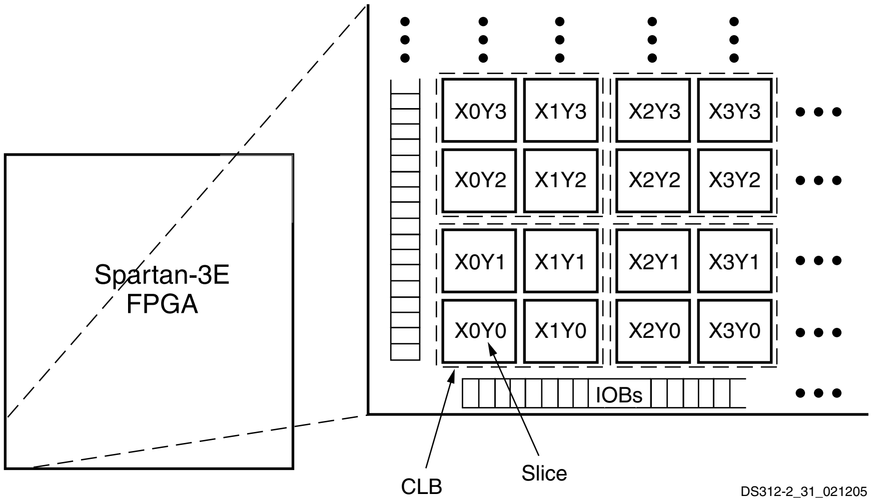


Figure 15: **CLB Locations**

Table 9: **Spartan-3E CLB Resources**

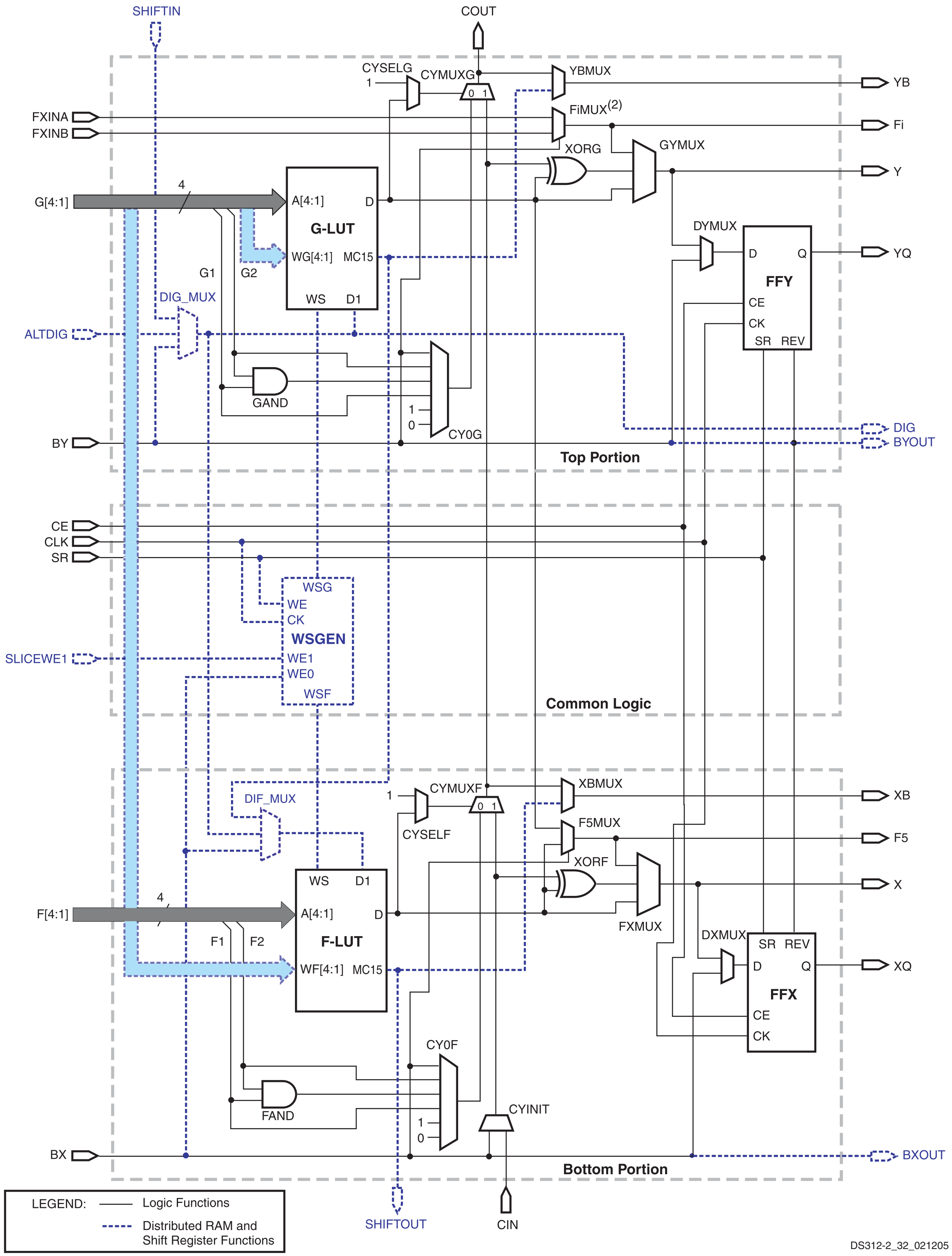
Device	CLB Rows	CLB Columns	CLB Total[1]	Slices	LUTs / Flip-Flops	Equivalent Logic Cells	RAM16 / SRL16	Distributed RAM Bits
XC3S100E	22	16	240	960	1920	2160	960	15360
XC3S250E	34	26	612	2448	4896	5508	2448	39168
XC3S500E	46	34	1164	4656	9312	10476	4656	74496
XC3S1200E	60	46	2168	8672	17344	19512	8672	138752
XC3S1600E	76	58	3688	14752	29504	33192	14752	236032

Notes:

1. The number of CLBs is less than the multiple of the rows and columns because the block RAM/multiplier blocks and the DCMs are embedded in the array (see Figure 1 in Module 1).

Slices

Each CLB comprises four interconnected slices, as shown in Figure 17. These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain. The left pair supports both logic and memory functions and its slices are called SLICEM. The right pair supports logic only and its slices are called SLICEL. Therefore half the LUTs support both logic and memory (including both RAM16 and SRL16 shift registers) while half support logic only, and the two types alternate throughout the array columns. The SLICEL reduces the size of the CLB and lowers the cost of the device, and can also provide a performance advantage over the SLICEM.



Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. The upper SLICEL has an F8MUX, and the upper SLICEM has an F7MUX. The lower SLICEL and SLICEM both have an F6MUX.

Figure 16: **Simplified Diagram of the Left-Hand SLICEM**

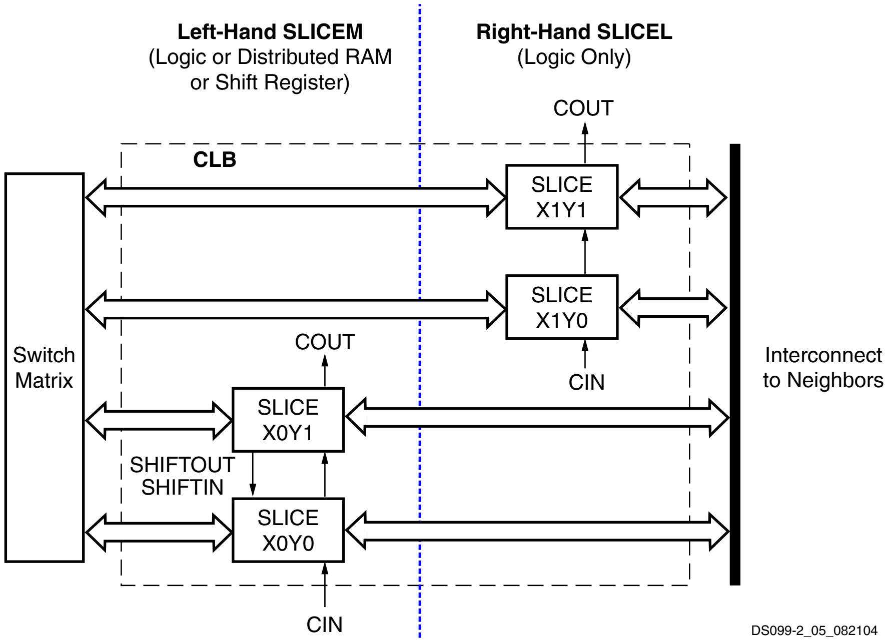


Figure 17: **Arrangement of Slices within the CLB**

Slice Location Designations

The Xilinx development software designates the location of a slice according to its X and Y coordinates, starting in the bottom left corner, as shown in Figure 15. The letter 'X' followed by a number identifies columns of slices, incrementing from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row, incrementing from the bottom of the die. Figure 17 shows the CLB located in the lower left-hand corner of the die. The SLICEM always has an even 'X' number, and the SLICEL always has an odd 'X' number.

Slice Overview

A slice includes two LUT function generators and two storage elements, along with additional logic, as shown in Figure 18.

Both SLICEM and SLICEL have the following elements in common to provide logic, arithmetic, and ROM functions:

- Two 4-input LUT function generators, F and G
- Two storage elements
- Two wide-function multiplexers, F5MUX and FiMUX
- Carry and arithmetic logic

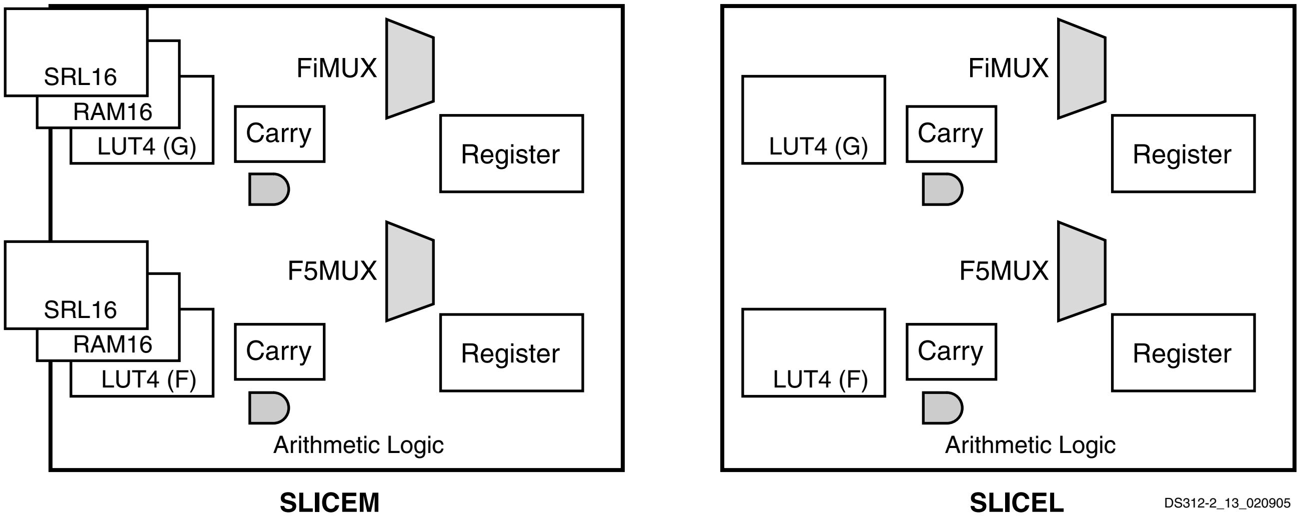


Figure 18: **Resources in a Slice**

The SLICEM pair supports two additional functions:

- Two 16x1 distributed RAM blocks, RAM16
- Two 16-bit shift registers, SRL16

Each of these elements is described in more detail in the following sections.

Logic Cells

The combination of a LUT and a storage element is known as a “Logic Cell”. The additional features in a slice, such as the wide multiplexers, carry logic, and arithmetic gates, add to the capacity of a slice, implementing logic that would otherwise require additional LUTs. Benchmarks have shown that the overall slice is equivalent to 2.25 simple logic cells. This calculation provides the equivalent logic cell count shown in Table 9.

Slice Details

Figure 20 is a detailed diagram of the SLICEM. It represents a superset of the elements and connections to be found in all slices. The dashed and gray lines (blue when viewed in color) indicate the resources found only in the SLICEM and not in the SLICEL.

Each slice has two halves, which are differentiated as top and bottom to keep them distinct from the upper and lower slices in a CLB. The control inputs for the clock (CLK), Clock Enable (CE), Slice Write Enable (SLICEWE1), and Reset/Set (RS) are shared in common between the two halves.

The LUTs located in the top and bottom portions of the slice are referred to as "G" and "F", respectively, or the "G-LUT" and the "F-LUT". The storage elements in the top and bottom portions of the slice are called FFY and FFX, respectively.

Each slice has two multiplexers with F5MUX in the bottom portion of the slice and FiMUX in the top portion. Depending on the slice, the FiMUX takes on the name F6MUX, F7MUX, or F8MUX, according to its position in the multiplexer chain. The lower SLICEL and SLICEM both have an F6MUX. The upper SLICEM has an F7MUX, and the upper SLICEL has an F8MUX.

The carry chain enters the bottom of the slice as CIN and exits at the top as COUT. Five multiplexers control the chain: CYINIT, CY0F, and CYMUXF in the bottom portion and CY0G and CYMUXG in the top portion. The dedicated arithmetic logic includes the exclusive-OR gates XORF and XORG (bottom and top portions of the slice, respectively) as well as the AND gates FAND and GAND (bottom and top portions, respectively).

See Table 10 for a description of all the slice input and output signals.

Table 10: **Slice Inputs and Outputs**

Name	Location	Direction	Description
F[4:1]	SLICEL/M Bottom	Input	F-LUT and FAND inputs
G[4:1]	SLICEL/M Top	Input	G-LUT and GAND inputs or Write Address (SLICEM)
BX	SLICEL/M Bottom	Input	Bypass to or output (SLICEM) or storage element, or control input to F5MUX, input to carry logic, or data input to RAM (SLICEM)
BY	SLICEL/M Top	Input	Bypass to or output (SLICEM) or storage element, or control input to FiMUX, input to carry logic, or data input to RAM (SLICEM)
BXOUT	SLICEM Bottom	Output	BX bypass output
BYOUT	SLICEM Top	Output	BY bypass output
ALTDIG	SLICEM Top	Input	Alternate data input to RAM
DIG	SLICEM Top	Output	ALTDIG or SHIFTIN bypass output
SLICEWE1	SLICEM Common	Input	RAM Write Enable
F5	SLICEL/M Bottom	Output	Output from F5MUX; direct feedback to FiMUX
FXINA	SLICEL/M Top	Input	Input to FiMUX; direct feedback from F5MUX or another FiMUX
FXINB	SLICEL/M Top	Input	Input to FiMUX; direct feedback from F5MUX or another FiMUX
Fi	SLICEL/M Top	Output	Output from FiMUX; direct feedback to another FiMUX
CE	SLICEL/M Common	Input	FFX/Y Clock Enable
SR	SLICEL/M Common	Input	FFX/Y Set or Reset or RAM Write Enable (SLICEM)

Table 10: **Slice Inputs and Outputs *(Continued)***

Name	Location	Direction	Description
CLK	SLICEL/M Common	Input	FFX/Y Clock or RAM Clock (SLICEM)
SHIFTIN	SLICEM Top	Input	Data input to G-LUT RAM
SHIFTOUT	SLICEM Bottom	Output	Shift data output from F-LUT RAM
CIN	SLICEL/M Bottom	Input	Carry chain input
COUT	SLICEL/M Top	Output	Carry chain output
X	SLICEL/M Bottom	Output	Combinatorial output
Y	SLICEL/M Top	Output	Combinatorial output
XB	SLICEL/M Bottom	Output	Combinatorial output from carry or F-LUT SRL16 (SLICEM)
YB	SLICEL/M Top	Output	Combinatorial output from carry or G-LUT SRL16 (SLICEM)
XQ	SLICEL/M Bottom	Output	FFX output
YQ	SLICEL/M Top	Output	FFY output

Main Logic Paths

Central to the operation of each slice are two nearly identical data paths at the top and bottom of the slice. The description that follows uses names associated with the bottom path. (The top path names appear in parentheses.) The basic path originates at an interconnect switch matrix outside the CLB. See **Interconnect** for more information on the switch matrix and the routing connections.

Four lines, F1 through F4 (or G1 through G4 on the upper path), enter the slice and connect directly to the LUT. Once inside the slice, the lower 4-bit path passes through a LUT ‘F’ (or ‘G’) that performs logic operations. The LUT Data output, ‘D’, offers five possible paths:

1. Exit the slice via line "X" (or "Y") and return to interconnect.
2. Inside the slice, "X" (or "Y") serves as an input to the DXMUX (or DYMUX) which feeds the data input, "D", of the FFX (or FFY) storage element. The "Q" output of the storage element drives the line XQ (or YQ) which exits the slice.
3. Control the CYMUXF (or CYMUXG) multiplexer on the carry chain.
4. With the carry chain, serve as an input to the XORF (or XORG) exclusive-OR gate that performs arithmetic operations, producing a result on "X" (or "Y").
5. Drive the multiplexer F5MUX to implement logic functions wider than four bits. The "D" outputs of both the F-LUT and G-LUT serve as data inputs to this multiplexer.

In addition to the main logic paths described above, there are two bypass paths that enter the slice as BX and BY. Once inside the FPGA, BX in the bottom half of the slice (or BY in the top half) can take any of several possible branches:

1. Bypass both the LUT and the storage element, and then exit the slice as BXOUT (or BYOUT) and return to interconnect.
2. Bypass the LUT, and then pass through a storage element via the D input before exiting as XQ (or YQ).
3. Control the wide function multiplexer F5MUX (or FiMUX).
4. Via multiplexers, serve as an input to the carry chain.
5. Drive the DI input of the LUT.
6. BY can control the REV inputs of both the FFY and FFX storage elements. See **Storage Element Functions**.
7. Finally, the DIG_MUX multiplexer can switch BY onto the DIG line, which exits the slice.

The control inputs CLK, CE, SR, BX and BY have programmable polarity. The LUT inputs do not need programmable polarity because their function can be inverted inside the LUT.

The sections that follow provide more detail on individual functions of the slice.

Look-Up Tables

The Look-Up Table or LUT is a RAM-based function generator and is the main resource for implementing logic functions. Furthermore, the LUTs in each SLICEM pair can be configured as Distributed RAM or a 16-bit shift register, as described later.

Each of the two LUTs (F and G) in a slice have four logic inputs (A1-A4) and a single output (D). Any four-variable Boolean logic operation can be implemented in one LUT. Functions with more inputs can be implemented by cascading LUTs or by using the wide function multiplexers that are described later.

The output of the LUT can connect to the wide multiplexer logic, the carry and arithmetic logic, or directly to a CLB output or to the CLB storage element. See Figure 19.

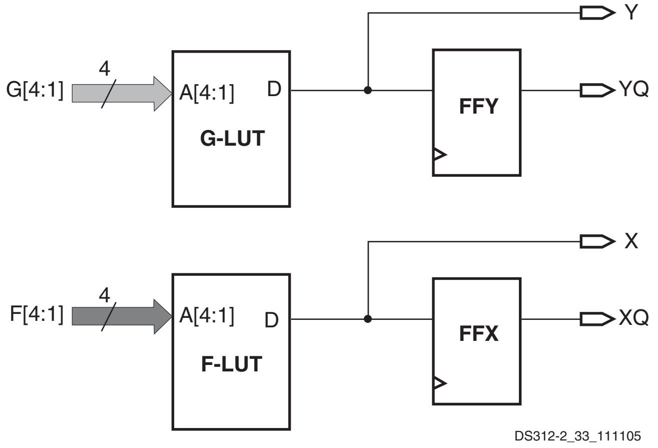


Figure 19: **LUT Resources in a Slice**

Wide Multiplexers

Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations. Each slice has two of these multiplexers with F5MUX in the bottom portion of the slice and FiMUX in the top portion. The F5MUX multiplexes the two LUTs in a slice. The FiMUX multiplexes two CLB inputs which connect directly to the F5MUX and FiMUX results from the same slice or from other slices. See Figure 20.

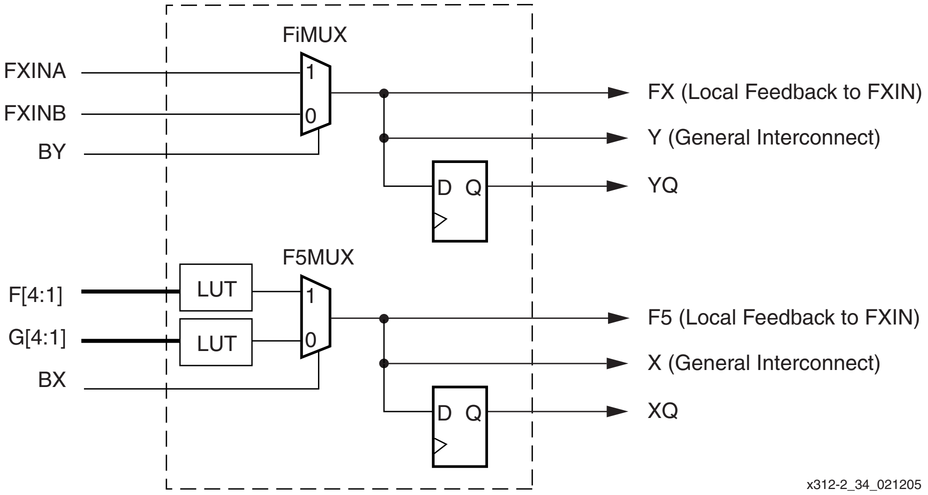


Figure 20: **Dedicated Multiplexers in Spartan-3E CLB**

Depending on the slice, FiMUX takes on the name F6MUX, F7MUX, or F8MUX. The designation indicates the number of inputs possible without restriction on the function. For example, an F7MUX can generate any function of seven inputs. Figure 21 shows the names of the multiplexers in each position in the Spartan-3E CLB. The figure also includes the direct connections within the CLB, along with the F7MUX connection to the CLB below.

Each mux can create logic functions of more inputs than indicated by its name. The F5MUX, for example, can generate any function of five inputs, with four inputs duplicated to two LUTs and the fifth input controlling the mux. Because each LUT can implement independent 2:1 muxes, the F5MUX can combine them to create a 4:1 mux, which is a six-input function. If the two LUTs have completely independent sets of inputs, some functions of all nine inputs can be implemented. Table 11 shows the connections for each multiplexer and the number of inputs possible for different types of functions.

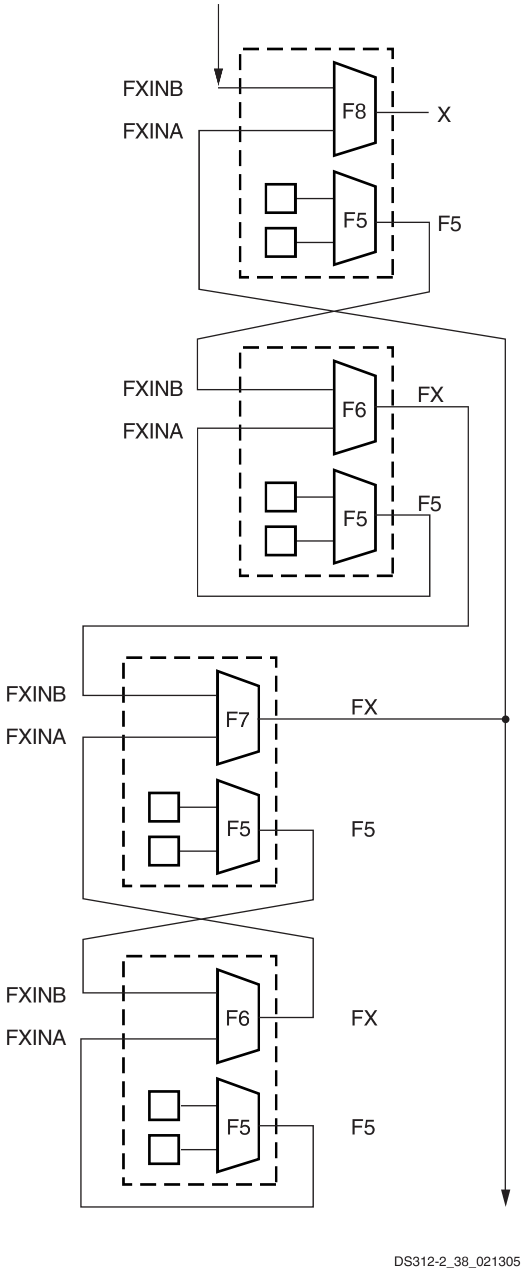


Figure 21: **Muxes and Dedicated Feedback in Spartan-3E CLB**

Table 11: **Mux Capabilities**

Mux	**Usage**	**Input Source**	**Total Number of Inputs per Function**		
			For Any Function	**For Mux**	**For Limited Functions**
F5MUX	F5MUX	LUTs	5	6 (4:1 mux)	9
FiMUX	F6MUX	F5MUX	6	11 (8:1 mux)	19
	F7MUX	F6MUX	7	20 (16:1 mux)	39
	F8MUX	F7MUX	8	37 (32:1 mux)	79

The wide multiplexers can be used by the automatic tools or instantiated in a design using a component such as the F5MUX. The symbol, signals, and function are described below. The description is similar for the F6MUX, F7MUX, and F8MUX. Each has versions with a general output, local output, or both.

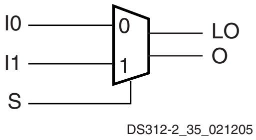


Figure 22: **F5MUX with Local and General Outputs**

Table 12: **F5MUX Inputs and Outputs**

Signal	Function
I0	Input selected when S is Low
I1	Input selected when S is High
S	Select input
LO	Local Output that connects to the F5 or FX CLB pins, which use local feedback to the FXIN inputs to the FiMUX for cascading
O	General Output that connects to the general-purpose combinatorial or registered outputs of the CLB

Table 13: **F5MUX Function**

Inputs			Outputs	
S	**I0**	**I1**	**O**	**LO**
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

For more details on using the multiplexers, see XAPP466: *Using Dedicated Multiplexers in Spartan-3 FPGAs*.

Carry and Arithmetic Logic

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry logic is automatically used for most arithmetic functions in a design. The gates and multiplexers of the carry and arithmetic logic can also be used for general-purpose logic, including simple wide Boolean functions.

The carry chain enters the slice as CIN and exits as COUT, controlled by several multiplexers. The carry chain connects directly from one CLB to the CLB above. The carry chain can be initialized at any point from the BX (or BY) inputs.

The dedicated arithmetic logic includes the exclusive-OR gates XORF and XORG (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). These gates work in conjunction with the LUTs to implement efficient arithmetic functions, including counters and multipliers, typically at two bits per slice. See Figure 23 and Table 14.

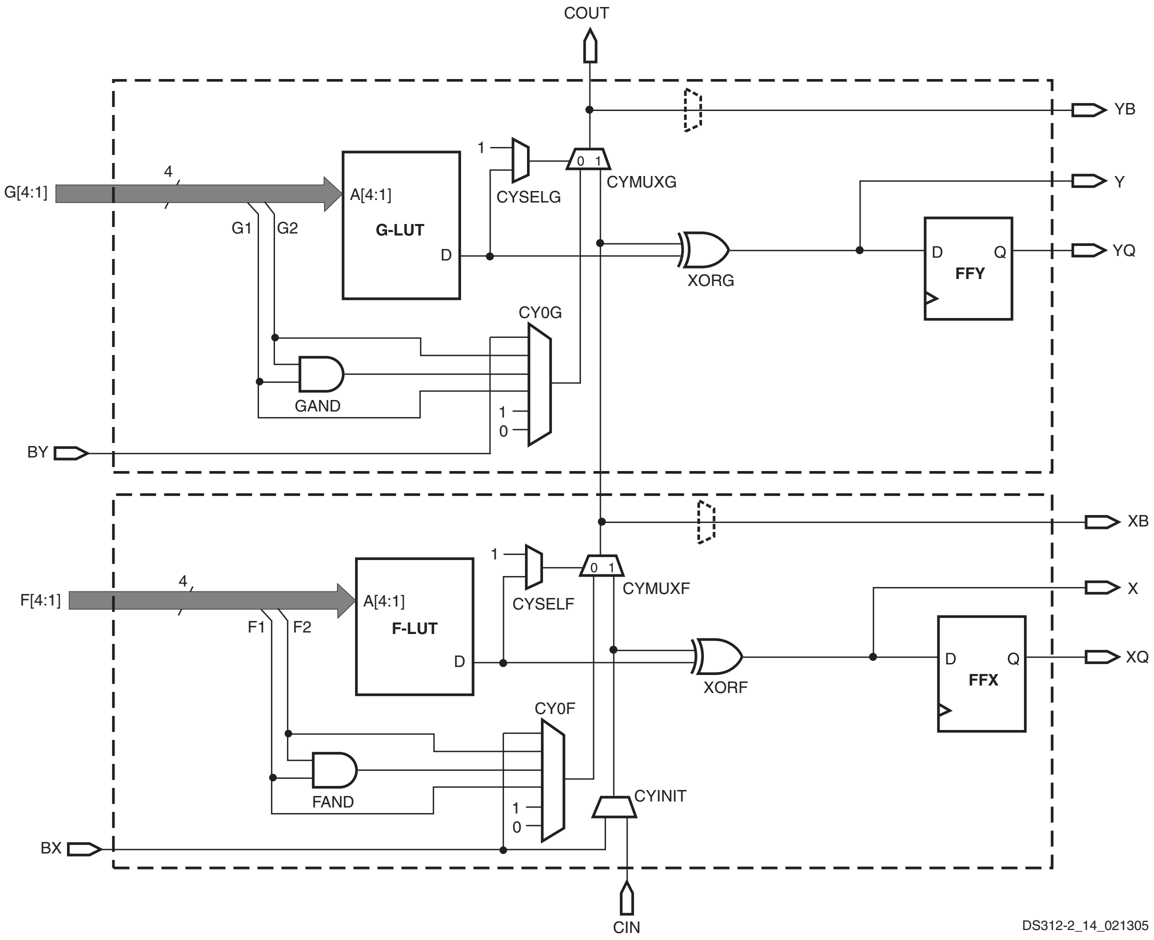


Figure 23: **Carry Logic**

Table 14: **Carry Logic Functions**

Function	Description
CYINIT	Initializes carry chain for a slice. Fixed selection of: • CIN carry input from the slice below • BX input
CY0F	Carry generation for bottom half of slice. Fixed selection of: • F1 or F2 inputs to the LUT (both equal 1 when a carry is to be generated) • FAND gate for multiplication • BX input for carry initialization • Fixed "1" or "0" input for use as a simple Boolean function
CY0G	Carry generation for top half of slice. Fixed selection of: • G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated) • GAND gate for multiplication • BY input for carry initialization • Fixed "1" or "0" input for use as a simple Boolean function
CYMUXF	Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of: • CYINIT carry propagation (CYSELF = 1) • CY0F carry generation (CYSELF = 0)

Table 14: **Carry Logic Functions *(Continued)***

Function	Description
CYMUXG	Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of: • CYMUXF carry propagation (CYSELG = 1) • CY0G carry generation (CYSELG = 0)
CYSELF	Carry generation or propagation select for bottom half of slice. Fixed selection of: • F-LUT output (typically XOR result) • Fixed "1" to always propagate
CYSELG	Carry generation or propagation select for top half of slice. Fixed selection of: • G-LUT output (typically XOR result) • Fixed "1" to always propagate
XORF	Sum generation for bottom half of slice. Inputs from: • F-LUT • CYINIT carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
XORG	Sum generation for top half of slice. Inputs from: • G-LUT • CYMUXF carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
FAND	Multiplier partial product for bottom half of slice. Inputs: • F-LUT F1 input • F-LUT F2 input Result is sent through CY0F to become the carry generate signal into CYMUXF
GAND	Multiplier partial product for top half of slice. Inputs: • G-LUT G1 input • G-LUT G2 input Result is sent through CY0G to become the carry generate signal into CYMUXG

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 24. The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 25.

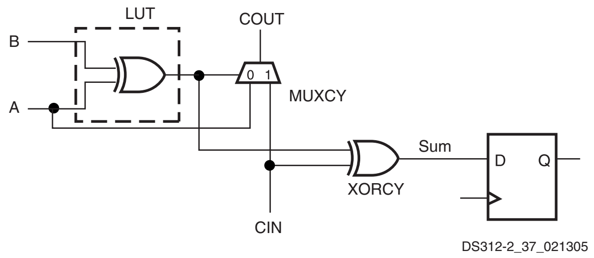


Figure 24: **Using the MUXCY and XORCY in the Carry Logic**

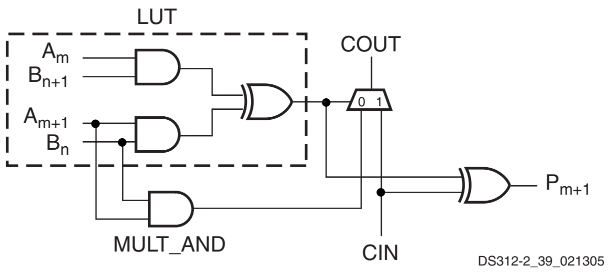


Figure 25: **Using the MULT_AND for Multiplication in Carry Logic**

The MULT_AND is useful for small multipliers. Larger multipliers can be built using the dedicated 18x18 multiplier blocks (see **Dedicated Multipliers**).

Storage Elements

The storage element, which is programmable as either a D-type flip-flop or a level-sensitive transparent latch, provides a means for synchronizing data to a clock signal, among other uses. The storage elements in the top and bottom portions of the slice are called FFY and FFX, respectively. FFY has a fixed multiplexer on the D input selecting either the combinatorial output Y or the bypass signal BY. FFX selects between the combinatorial output X or the bypass signal BX.

The functionality of a slice storage element is identical to that described earlier for the I/O storage elements. All signals have programmable polarity; the default active-High function is described.

Table 15: **Storage Element Signals**

Signal	Description
D	Input. For a flip-flop data on the D input is loaded when R and S (or CLR and PRE) are Low and CE is High during the Low-to-High clock transition. For a latch, Q reflects the D input while the gate (G) input and gate enable (GE) are High and R and S (or CLR and PRE) are Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output of the latch remains unchanged as long as G or GE remains Low.
Q	Output. Toggles after the Low-to-High clock transition for a flip-flop and immediately for a latch.
C	Clock for edge-triggered flip-flops.
G	Gate for level-sensitive latches.
CE	Clock Enable for flip-flops.
GE	Gate Enable for latches.
S	Synchronous Set (Q = High). When the S input is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. A latch output is immediately set, output High.
R	Synchronous Reset (Q = Low); has precedence over Set.
PRE	Asynchronous Preset (Q = High). When the PRE input is High and CLR is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. A latch output is immediately set, output High.
CLR	Asynchronous Clear (Q = Low); has precedence over Preset to reset Q output Low
SR	CLB input for R, S, CLR, or PRE
REV	CLB input for opposite of SR. Must be asynchronous or synchronous to match SR.

The control inputs R, S, CE, and C are all shared between the two flip-flops in a slice.

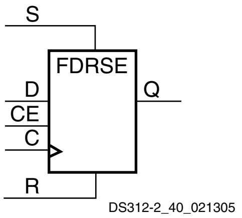


Figure 26: **FD Flip-Flop Component with Synchronous Reset, Set, and Clock Enable**

Table 16: **FD Flip-Flop Functionality with Synchronous Reset, Set, and Clock Enable**

Inputs					Outputs
R	**S**	**CE**	**D**	**C**	**Q**
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Change
0	0	1	1	↑	1
0	0	1	0	↑	0

Initialization

The CLB storage elements are initialized at power-up, during configuration, by the global GSR signal, and by the individual SR or REV inputs to the CLB. The storage elements can also be re-initialized using the GSR input on the STARTUP_SPARTAN3E primitive. See **Global Controls (STARTUP_SPARTAN3E)**.

Table 17: **Slice Storage Element Initialization**

Signal	Description
SR	Set/Reset input. Forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic “1” when SR is asserted. SRLOW forces a logic “0”. For each slice, set and reset can be set to be synchronous or asynchronous.
REV	Reverse of Set/Reset input. A second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition if both are active. Same synchronous/asynchronous setting as for SR.
GSR	Global Set/Reset. GSR defaults to active High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN3E element. The initial state after configuration or GSR is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1.

Distributed RAM

The LUTs in the SLICEM can be programmed as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One SLICEM LUT stores 16 bits (RAM16). The four LUT inputs F[4:1] or G[4:1] become the address lines labeled A[4:1] in the device model and A[3:0] in the design components, providing a 16x1 configuration in one LUT. Multiple SLICEM LUTs can be combined in various ways to store larger amounts of data, including 16x4, 32x2, or 64x1 configurations in one CLB. The fifth and sixth address lines required for the 32-deep and 64-deep configurations, respectively, are implemented using the BX and BY inputs, which connect to the write enable logic for writing and the F5MUX and F6MUX for reading.

Writing to distributed RAM is always synchronous to the SLICEM clock (WCLK for distributed RAM) and enabled by the SLICEM SR input which functions as the active-High Write Enable (WE). The read operation is asynchronous, and, therefore, during a write, the output initially reflects the old data at the address being written.

The distributed RAM outputs can be captured using the flip-flops within the SLICEM element. The WE write-enable control for the RAM and the CE clock-enable control for the flip-flop are independent, but the WCLK and CLK clock inputs are shared. Because the RAM read operation is asynchronous, the output data always reflects the currently addressed RAM location.

A dual-port option combines two LUTs so that memory access is possible from two independent data lines. The same data is written to both 16x1 memories but they have independent read address lines and outputs. The dual-port function is implemented by cascading the G-LUT address lines, which are used for both read and write, to the F-LUT write address lines (WF[4:1] in Figure 16), and by cascading the G-LUT data input D1 through the DIF_MUX in Figure 16 and to the D1 input on the F-LUT. One CLB provides a 16x1 dual-port memory as shown in Figure 27.

Any write operation on the D input and any read operation on the SPO output can occur simultaneously with and independently from a read operation on the second read-only port, DPO.

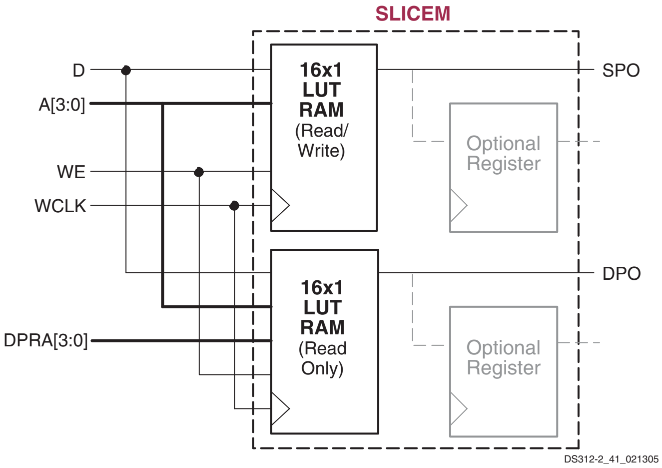


Figure 27: **RAM16X1D Dual-Port Usage**

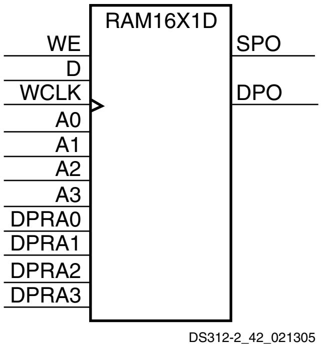


Figure 28: **Dual-Port RAM Component**

Table 18: **Dual-Port RAM Function**

Inputs			**Outputs**	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Notes:

1. data_a = word addressed by bits A3-A0.
2. data_d = word addressed by bits DPRA3-DPRA0.

Table 19: **Distributed RAM Signals**

Signal	**Description**
WCLK	The clock is used for synchronous writes. The data and the address input pins have setup times referenced to the WCLK pin. Active on the positive edge by default with built-in programmable polarity.
WE	The enable pin affects the write functionality of the port. An inactive Write Enable prevents any writing to memory cells. An active Write Enable causes the clock edge to write the data input signal to the memory location pointed to by the address inputs. Active High by default with built-in programmable polarity.
A0, A1, A2, A3 (A4, A5)	The address inputs select the memory cells for read or write. The width of the port determines the required address inputs.
D	The data input provides the new data value to be written into the RAM.
O, SPO, and DPO	The data output O on single-port RAM or the SPO and DPO outputs on dual-port RAM reflects the contents of the memory cells referenced by the address inputs. Following an active write clock edge, the data out (O or SPO) reflects the newly written data.

The INIT attribute can be used to preload the memory with data during FPGA configuration. The default initial contents for RAM is all zeros. If the WE is held Low, the element can be considered a ROM. The ROM function is possible even in the SLICEL.

The global write enable signal, GWE, is asserted automatically at the end of device configuration to enable all writable elements. The GWE signal guarantees that the initialized distributed RAM contents are not disturbed during the configuration process.

The distributed RAM is useful for smaller amounts of memory. Larger memory requirements can use the dedicated 18Kbit RAM blocks (see **Block RAM**).

For more information on distributed RAM, see XAPP464: *Using Look-Up Tables as Distributed RAM in Spartan-3 FPGAs*.

Shift Registers

It is possible to program each SLICEM LUT as a 16-bit shift register (see Figure 29). Used in this way, each LUT can delay serial data anywhere from 1 to 16 clock cycles without using any of the dedicated flip-flops. The resulting programmable delays can be used to balance the timing of data pipelines.

The SLICEM LUTs cascade from the G-LUT to the F-LUT through the DIFMUX (see Figure 16). SHIFTIN and SHIFTOUT lines cascade a SLICEM to the SLICEM below to form larger shift registers. The four SLICEM LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. It is also possible to combine shift registers across more than one CLB.

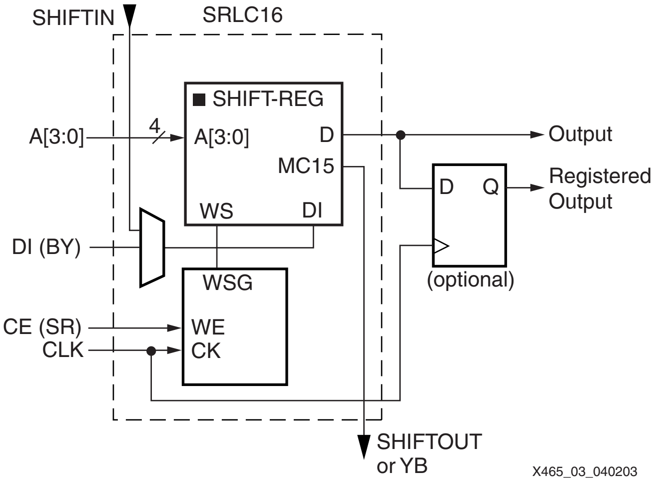


Figure 29: **Logic Cell SRL16 Structure**

Each shift register provides a shift output MC15 for the last bit in each LUT, in addition to providing addressable access to any bit in the shift register through the normal D output. The address inputs A[3:0] are the same as the distributed RAM address lines, which come from the LUT inputs F[4:1] or G[4:1]. At the end of the shift register, the CLB flip-flop can be used to provide one more shift delay for the addressable bit.

The shift register element is known as the SRL16 (Shift Register LUT 16-bit), with a 'C' added to signify a cascade ability (Q15 output) and 'E' to indicate a Clock Enable. See Figure 30 for an example of the SRLC16E component.

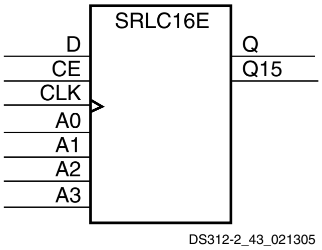


Figure 30: **SRL16 Shift Register Component with Cascade and Clock Enable**

The functionality of the shift register is shown in Table 20. The SRL16 shifts on the rising edge of the clock input when the Clock Enable control is High. This shift register cannot be initialized either during configuration or during operation except by shifting data into it. The clock enable and clock inputs are shared between the two LUTs in a SLICEM. The clock enable input is automatically kept active if unused.

Table 20: **SRL16 Shift Register Function**

Inputs				Outputs	
Am	**CLK**	**CE**	**D**	**Q**	**Q15**
Am	X	0	X	Q[Am]	Q[15]
Am	↑	1	D	Q[Am-1]	Q[15]

Notes:

1. m = 0, 1, 2, 3.

For more information on the SRL16, refer to XAPP465: *Using Look-Up Tables as Shift Registers (SRL16) in Spartan-3 FPGAs*.

Block RAM

Spartan-3E devices incorporate 4 to 36 dedicated block RAMs, which are organized as dual-port configurable 18 Kbit blocks. Functionally, the block RAM is identical to the Spartan-3 architecture block RAM. Block RAM synchronously stores large amounts of data while distributed RAM, previously described, is better suited for buffering small amounts of data anywhere along signal paths. This section describes basic block RAM functions. For detailed implementation information, refer to XAPP463: *Using Block RAM in Spartan-3 Series FPGAs*.

Each block RAM is configurable by setting the content's initial values, default signal value of the output registers, port aspect ratios, and write modes. Block RAM can be used in single-port or dual-port modes.

Arrangement of RAM Blocks on Die

The block RAMs are located together with the multipliers on the die in one or two columns depending on the size of the device. The XC3S100E has one column of block RAM. The Spartan-3E devices ranging from the XC3S250E to XC3S1600E have two columns of block RAM. Table 21 shows the number of RAM blocks, the data storage capacity, and the number of columns for each device. Row(s) of CLBs are located above and below each block RAM column.

Table 21: **Number of RAM Blocks by Device**

Device	Total Number of RAM Blocks	Total Addressable Locations (bits)	Number of Columns
XC3S100E	4	73,728	1
XC3S250E	12	221,184	2
XC3S500E	20	368,640	2
XC3S1200E	28	516,096	2
XC3S1600E	36	663,552	2

Immediately adjacent to each block RAM is an embedded 18x18 hardware multiplier. The upper 16 bits of the block RAM's Port A Data input bus are shared with the upper 16 bits of the A multiplicand input bus of the multiplier. Similarly, the upper 16 bits of Port B's data input bus are shared with the B multiplicand input bus of the multiplier.

The Internal Structure of the Block RAM

The block RAM has a dual port structure. The two identical data ports called A and B permit independent access to the common block RAM, which has a maximum capacity of 18,432 bits, or 16,384 bits with no parity bits (see parity bits description in Table 22). Each port has its own dedicated set of data, control, and clock lines for synchronous read and write operations. There are four basic data paths, as shown in Figure 31:

1. Write to and read from Port A
2. Write to and read from Port B
3. Data transfer from Port A to Port B
4. Data transfer from Port B to Port A

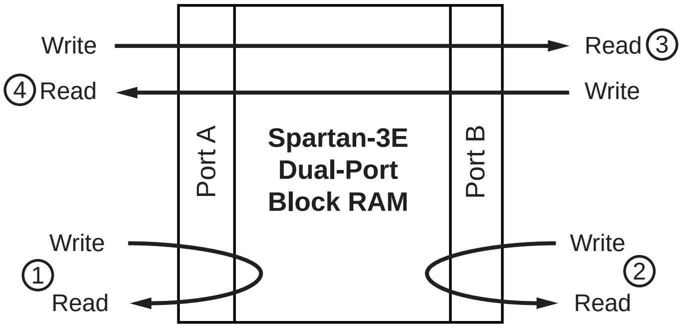


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Figure 31: **Block RAM Data Paths**

Number of Ports

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[w_A]_S[w_B] calls out the dual-port primitive, where the integers w_A and w_B specify the total data path width at ports A and B, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit Port A and an 18-bit Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port A. A RAMB16_S18 is a single-port RAM with an 18-bit port.

Port Aspect Ratios

Each port of the block RAM can be configured independently to select a number of different possible widths for the data input (DI) and data output (DO) signals as shown in Table 22.

Table 22: **Port Aspect Ratios**

Total Data Path Width (w bits)	DI/DO Data Bus Width (w-p bits)[1]	DIP/DOP Parity Bus Width (p bits)	ADDR Bus Width (r bits)[2]	DI/DO [w-p-1:0]	DIP/DOP [p-1:0]	ADDR [r-1:0]	No. of Addressable Locations (n)[3]	Block RAM Capacity (w*n bits)[4]
1	1	0	14	[0:0]	-	[13:0]	16,384	16,384
2	2	0	13	[1:0]	-	[12:0]	8,192	16,384
4	4	0	12	[3:0]	-	[11:0]	4,096	16,384
9	8	1	11	[7:0]	[0:0]	[10:0]	2,048	18,432
18	16	2	10	[15:0]	[1:0]	[9:0]	1,024	18,432
36	32	4	9	[31:0]	[3:0]	[8:0]	512	18,432

Notes:

1. The width of the total data path (w) is the sum of the DI/DO bus width (w-p) and any parity bits (p).
2. The width selection made for the DI/DO bus determines the number of address lines (r) according to the relationship expressed as: $r = 14 - [\log(w-p)/\log(2)]$.
3. The number of address lines delimits the total number (n) of addressable locations or depth according to the following equation: $n = 2^r$.
4. The product of w and n yields the total block RAM capacity.

If the data bus width of Port A differs from that of Port B, the block RAM automatically performs a bus-matching function as described in Figure 32. When data is written to a port with a narrow bus and then read from a port with a wide bus, the latter port effectively combines "narrow" words to form "wide" words. Similarly, when data is written into a port with a wide bus and then read from a port with a narrow bus, the latter port divides "wide" words to form "narrow" words. Parity bits are not available if the data port width is configured as x4, x2, or x1. For example, if a x36 data word (32 data, 4 parity) is addressed as two x18 halfwords (16 data, 2 parity), the parity bits associated with each data byte are mapped within the block RAM to the appropriate parity bits. The same effect happens when the x36 data word is mapped as four x9 words.

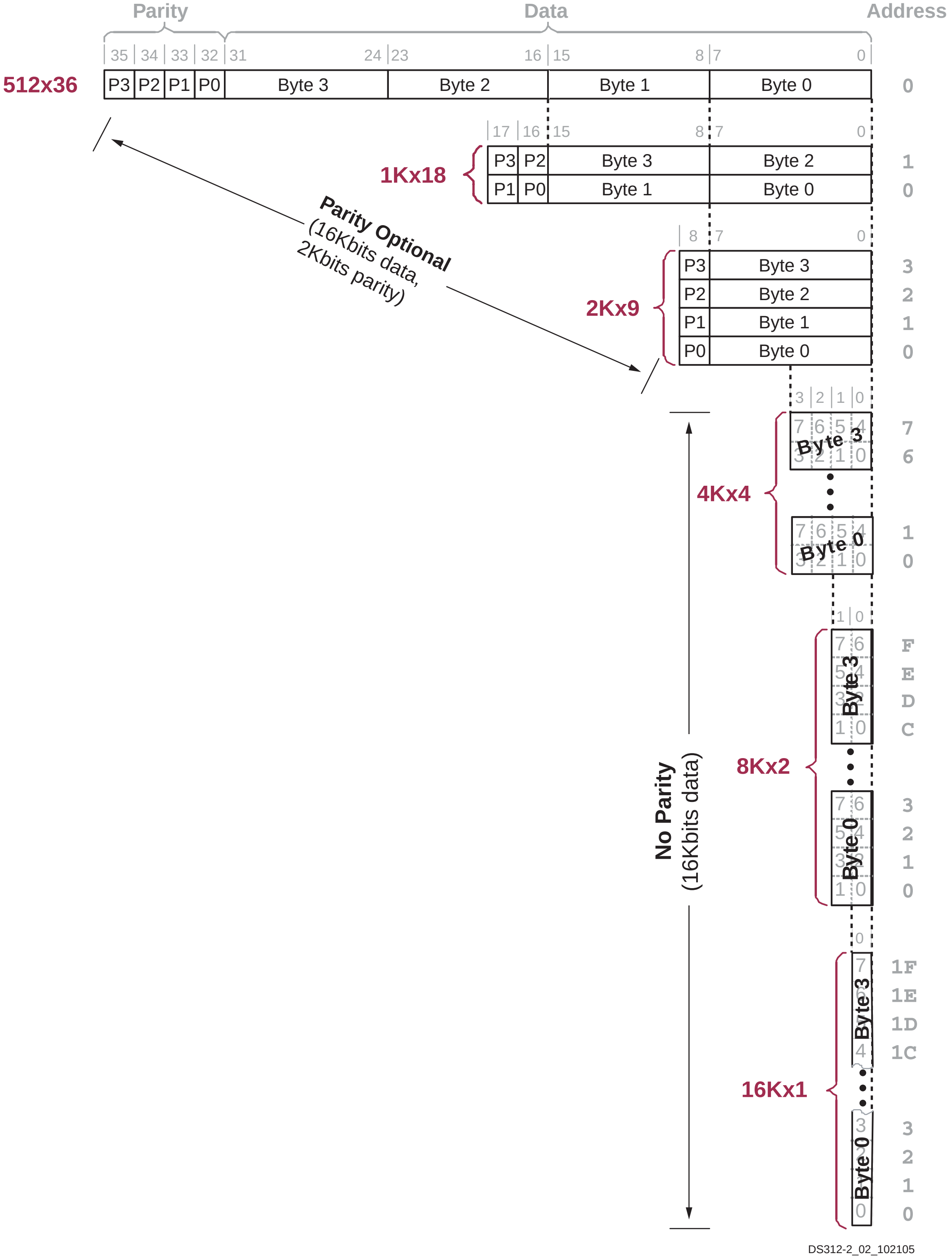


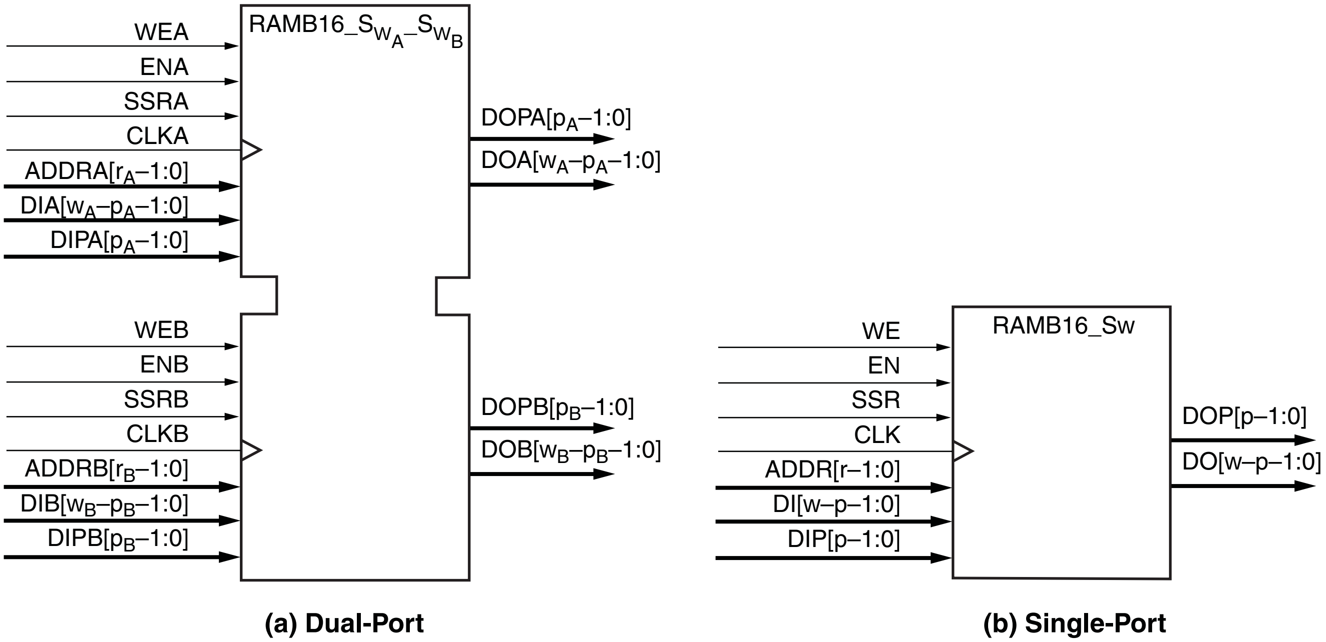
Figure 32: **Data Organization and Bus-matching Operation with Different Port Widths on Port A and Port B**

Block RAM Port Signal Definitions

Representations of the dual-port primitive RAMB16_S[w_A]_S[w_B] and the single-port primitive RAMB16_S[w] with their associated signals are shown in Figure 33a and Figure 33b, respectively. These signals are defined in Table 23. The control signals (WE, EN, CLK, and SSR) on the block RAM are active High. However, optional inverters on the control signals change the polarity of the active edge to active Low.

DESIGN NOTE:

⚠ Whenever a block RAM port is enabled (ENA or ENB = High), all address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB), as shown in Table 100, page 141.This requirement must be met even if the RAM read output is of no interest.



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Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at Ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 33: **Block RAM Primitives**

Table 23: **Block RAM Port Signals**

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r), as per Table 22. Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB), as shown in Table 100, page 141.This requirement must be met even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the RAM location specified by the address input bus (ADDR) during the active edge of the CLK input, when the clock enable (EN) and write enable (WE) inputs are active. It is possible to configure a port's DI input bus width (w-p) based on Table 22. This selection applies to both the DI and DO paths of a given port.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path. Although referred to herein as "parity" bits, the parity inputs and outputs have no special functionality for generating or checking parity and can be used as additional data bits. The number of parity bits 'p' included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 22.
Data Output Bus	DOA	DOB	Output	Data is written to the DO output bus from the RAM location specified by the address input bus, ADDR. See the DI signal description for DO port width configurations. Basic data access occurs on the active edge of the CLK when WE is inactive and EN is active. The DO outputs mirror the data stored in the address ADDR memory location. Data access with WE active if the WRITE_MODE attribute is set to the value: WRITE_FIRST, which accesses data after the write takes place. READ_FIRST accesses data before the write occurs. A third attribute, NO_CHANGE, latches the DO outputs upon the assertion of WE. See **Block RAM Data Operations** for details on the WRITE_MODE attribute.
Parity Data Output(s)	DOPA	DOPB	Output	Parity outputs represent additional bits included in the data input path. The number of parity bits 'p' included in the DI bus (same as for the DO bus) depends on a port's total data path width (w). See the DIP signal description for configuration details.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. When WE is inactive with EN asserted, read operations are still possible. In this case, a latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to perform read and write operations to the block RAM. When inactive, the block RAM does not perform any read or write operations.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value of the SRVAL attribute. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

Block RAM Attribute Definitions

A block RAM has a number of attributes that control its behavior as shown in Table 24.

Table 24: **Block RAM Attributes**

Function	Attribute	Possible Values
Initial Content for Data Memory, Loaded during Configuration	`INITxx` (INIT_00 through INIT3F)	Each initialization string defines 32 hex values of the 16384-bit data memory of the block RAM.
Initial Content for Parity Memory, Loaded during Configuration	`INITPxx` (INITP_00 through INITP0F)	Each initialization string defines 32 hex values of the 2048-bit parity data memory of the block RAM.
Data Output Latch Initialization	`INIT` (single-port) `INITA`, `INITB` (dual-port)	Hex value the width of the chosen port.
Data Output Latch Synchronous Set/Reset Value	`SRVAL` (single-port) `SRVAL_A`, `SRVAL_B` (dual-port)	Hex value the width of the chosen port.
Data Output Latch Behavior during Write (see **Block RAM Data Operations**)	`WRITE_MODE`	WRITE_FIRST, READ_FIRST, NO_CHANGE

Block RAM Data Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports. Table 25 describes the data operations of each port as a result of the block RAM control signals in their default active-High edges.

The waveforms for the write operation are shown in the top half of Figure 34, Figure 35, and Figure 36. When the WE and EN signals enable the active edge of CLK, data at the DI input bus is written to the block RAM location addressed by the ADDR lines.

Table 25: **Block RAM Function Table**

Input Signals								**Output Signals**		**RAM Data**	
GSR	**EN**	**SSR**	**WE**	**CLK**	**ADDR**	**DIP**	**DI**	**DOP**	**DO**	**Parity**	**Data**
Immediately After Configuration											
Loaded During Configuration								X	X	INITP_xx	INIT_xx
Global Set/Reset Immediately After Configuration											
1	X	X	X	X	X	X	X	INIT	INIT	No Chg	No Chg
RAM Disabled											
0	0	X	X	X	X	X	X	No Chg	No Chg	No Chg	No Chg
Synchronous Set/Reset											
0	1	1	0	↑	X	X	X	SRVAL	SRVAL	No Chg	No Chg
Synchronous Set/Reset During Write RAM											
0	1	1	1	↑	addr	pdata	Data	SRVAL	SRVAL	RAM(addr) ← pdata	RAM(addr) ← data
Read RAM, no Write Operation											
0	1	0	0	↑	addr	X	X	RAM(pdata)	RAM(data)	No Chg	No Chg

Table 25: **Block RAM Function Table *(Continued)***

Input Signals								Output Signals		RAM Data	
GSR	**EN**	**SSR**	**WE**	**CLK**	**ADDR**	**DIP**	**DI**	**DOP**	**DO**	**Parity**	**Data**
Write RAM, Simultaneous Read Operation											
0	1	0	1	↑	addr	pdata	Data	WRITE_MODE = WRITE_FIRST			
								pdata	data	RAM(addr) ← pdata	RAM(addr) ← data
								WRITE_MODE = READ_FIRST			
								RAM(data)	RAM(data)	RAM(addr) ← pdata	RAM(addr) ← pdata
								WRITE_MODE = NO_CHANGE			
								No Chg	No Chg	RAM(addr) ← pdata	RAM(addr) ← pdata

There are a number of different conditions under which data can be accessed at the DO outputs. Basic data access always occurs when the WE input is inactive. Under this condition, data stored in the memory location addressed by the ADDR lines passes through a output latch to the DO outputs. The timing for basic data access is shown in the portions of Figure 34, Figure 35, and Figure 36 during which WE is Low.

Data also can be accessed on the DO outputs when asserting the WE input based on the value of the WRITE_MODE attribute as described in Table 26.

Table 26: **WRITE_MODE Effect on Data Output Latches During Write Operations**

Write Mode	Effect on Same Port	Effect on Opposite Port (dual-port only with same address)
WRITE_FIRST Read After Write	Data on DI and DIP inputs is written into specified RAM location and simultaneously appears on DO and DOP outputs.	Invalidates data on DO and DOP outputs.
READ_FIRST Read Before Write	Data from specified RAM location appears on DO and DOP outputs. Data on DI and DIP inputs is written into specified location.	Data from specified RAM location appears on DO and DOP outputs.
NO_CHANGE No Read on Write	Data on DO and DOP outputs remains unchanged. Data on DI and DIP inputs is written into specified location.	Invalidates data on DO and DOP outputs.

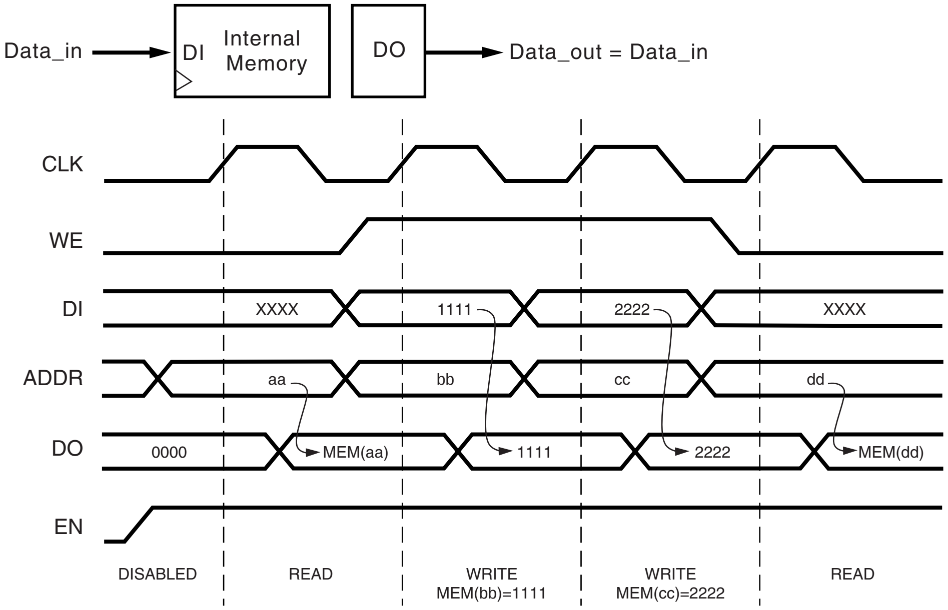

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Figure 34: **Waveforms of Block RAM Data Operations with WRITE_FIRST Selected**

Setting the WRITE_MODE attribute to a value of WRITE_FIRST, data is written to the addressed memory location on an enabled active CLK edge and is also passed to the DO outputs. WRITE_FIRST timing is shown in the portion of Figure 34 during which WE is High.

Setting the WRITE_MODE attribute to a value of READ_FIRST, data already stored in the addressed location passes to the DO outputs before that location is overwritten with new data from the DI inputs on an enabled active CLK edge. READ_FIRST timing is shown in the portion of Figure 35 during which WE is High.

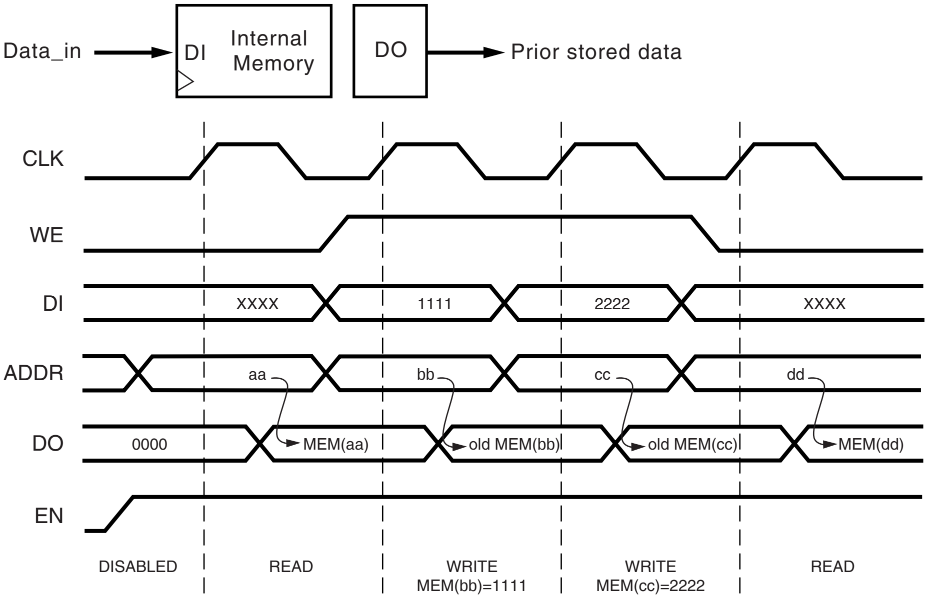

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Figure 35: **Waveforms of Block RAM Data Operations with READ_FIRST Selected**

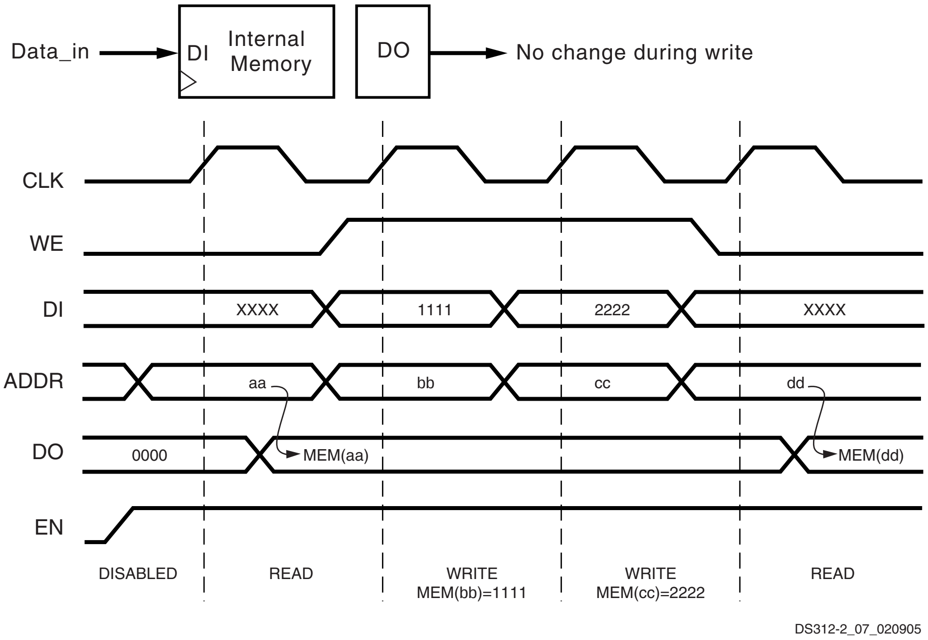


Figure 36: **Waveforms of Block RAM Data Operations with NO_CHANGE Selected**

Setting the WRITE_MODE attribute to a value of NO_CHANGE, puts the DO outputs in a latched state when asserting WE. Under this condition, the DO outputs retain the data driven just before WE is asserted. NO_CHANGE timing is shown in the portion of Figure 36 during which WE is High.

Dedicated Multipliers

The Spartan-3E devices provide 4 to 36 dedicated multiplier blocks per device. The multipliers are located together with the block RAM in one or two columns depending on device density. See **Arrangement of RAM Blocks on Die** for details on the location of these blocks and their connectivity.

Operation

The multiplier blocks primarily perform two's complement numerical multiplication but can also perform some less obvious applications, such as simple data storage and barrel shifting. Logic slices also implement efficient small multipliers and thereby supplement the dedicated multipliers. The Spartan-3E dedicated multiplier blocks have additional features beyond those provided in Spartan-3 FPGAs.

Each multiplier performs the principle operation P = A × B, where 'A' and 'B' are 18-bit words in two's complement form, and 'P' is the full-precision 36-bit product, also in two's complement form. The 18-bit inputs represent values ranging from $-131{,}072_{10}$ to $+131{,}071_{10}$ with a resulting product ranging from $-17{,}179{,}738{,}112_{10}$ to $+17{,}179{,}869{,}184_{10}$.

Implement multipliers with inputs less than 18 bits by sign-extending the inputs (i.e., replicating the most-significant bit). Wider multiplication operations are performed by combining the dedicated multipliers and slice-based logic in any viable combination or by time-sharing a single multiplier. Perform unsigned multiplication by restricting the inputs to the positive range. Tie the most-significant bit Low and represent the unsigned value in the remaining 17 lesser-significant bits.

Optional Pipeline Registers

As shown in Figure 37, each multiplier block has optional registers on each of the multiplier inputs and the output. The registers are named AREG, BREG, and PREG and can be used in any combination. The clock input is common to all the registers within a block, but each register has an independent clock enable and synchronous reset controls making them ideal for storing data samples and coefficients. When used for pipelining, the registers boost the multiplier clock rate, beneficial for higher performance applications.

Figure 37 illustrates the principle features of the multiplier block.

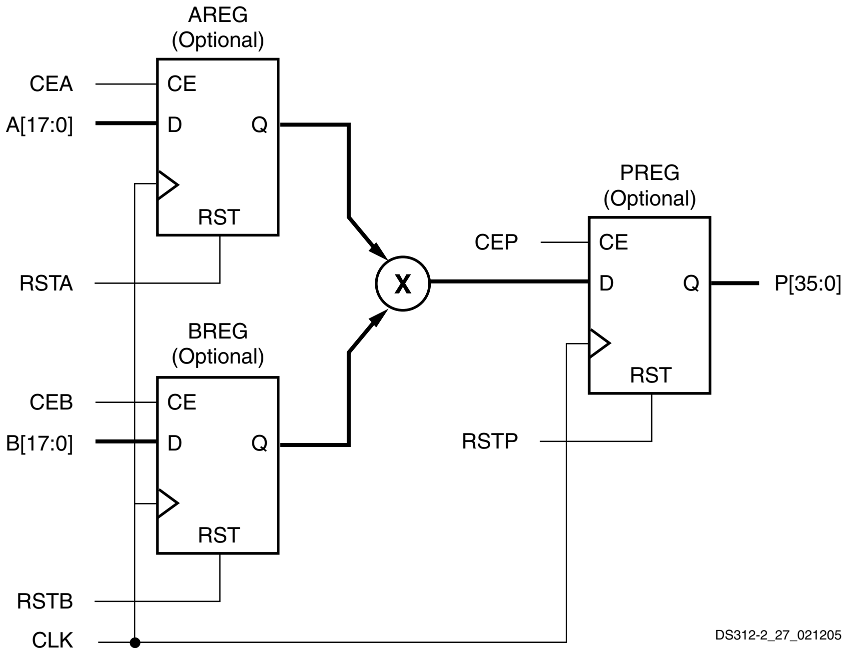


Figure 37: **Principle Ports and Functions of Dedicated Multiplier Blocks**

Use the MULT18X18SIO primitive shown in Figure 38 to instantiate a multiplier within a design. Although high-level logic synthesis software usually automatically infers a multiplier, adding the pipeline registers may require the MULT18X18SIO primitive. Connect the appropriate signals to the MULT18X18SIO multiplier ports and set the individual AREG, BREG, and PREG attributes to '1' to insert the associated register, or to 0 to remove it and make the signal path combinatorial.

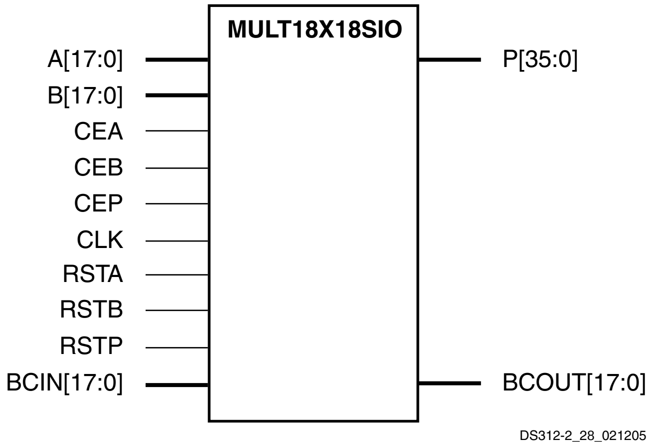


Figure 38: **MULT18X18SIO Primitive**

Cascading Multipliers

The MULT18X18SIO primitive has two additional ports called BCIN and BCOUT to cascade or share the multiplier's 'B' input among several multiplier bocks. The 18-bit BCIN "cascade" input port offers an alternate input source from the more typical 'B' input. The B_INPUT attribute specifies whether the specific implementation uses the BCIN or 'B' input path. Setting B_INPUT to DIRECT chooses the 'B' input. Setting B_INPUT to CASCADE selects the alternate BCIN input. The BREG register then optionally holds the selected input value, if required.

BCOUT is an 18-bit output port that always reflects the value that is applied to the multiplier's second input, which is either the 'B' input, the cascaded value from the BCIN input, or the output of the BREG if it is inserted.

Figure 39 illustrates the four possible configurations using different settings for the B_INPUT attribute and the BREG attribute.

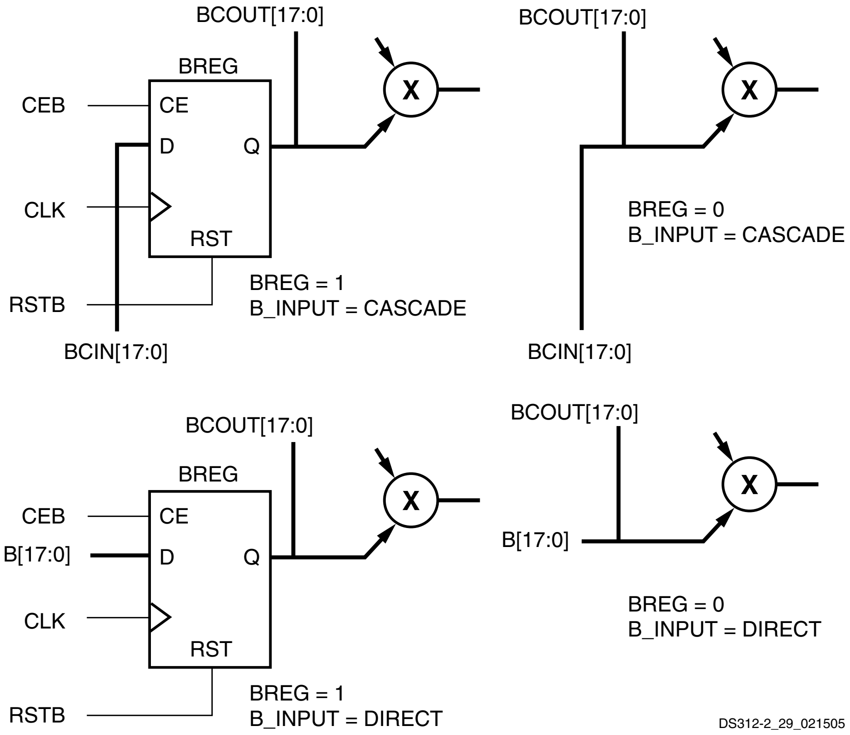


Figure 39: **Four Configurations of the B Input**

The BCIN and BCOUT ports have associated dedicated routing that connects adjacent multipliers within the same column. Via the cascade connection, the BCOUT port of one multiplier block drives the BCIN port of the multiplier block directly above it. There is no connection to the BCIN port of the bottom-most multiplier block in a column or a connection from the BCOUT port of the top-most block in a column. As an example, Figure 40 shows the multiplier cascade capability within the XC3S100E FPGA, which has a single column of multiplier, four blocks tall. For clarity, the figure omits the register control inputs.

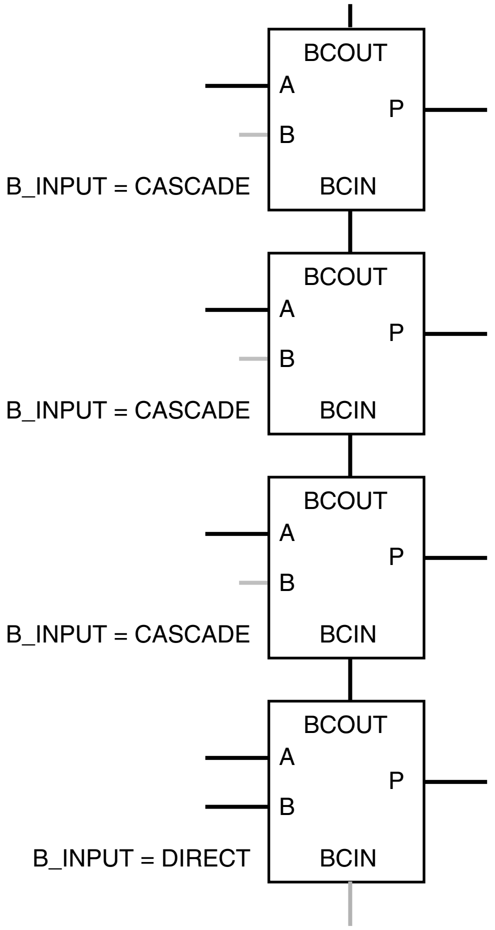


Figure 40: **Multiplier Cascade Connection**

When using the BREG register, the cascade connection forms a shift register structure typically used in DSP algorithms such as direct-form FIR filters. When the BREG register is omitted, the cascade structure essentially feeds the same input value to more than one multiplier. This parallel connection serves to create wide-input multipliers, implement transpose FIR filters, and is used in any application that requires that several multipliers have the same input value.

Multiplier/Block RAM Interaction

Each multiplier is located adjacent to an 18 Kbit block RAM and shares some interconnect resources. Configuring an 18 Kbit block RAM for 36-bit wide data (512 x 36 mode) prevents use of the associated dedicated multiplier.

The upper 16 bits of the ‘A’ multiplicand input are shared with the upper 16 bits of the block RAM’s Port A Data input. Similarly, the upper 16 bits of the ‘B’ multiplicand input are shared with Port B’s data input. See also Figure 49, page 64.

Table 27 defines each port of the MULT18X18SIO primitive.

Table 27: **MULT18X18SIO Embedded Multiplier Primitives Description**

Signal Name	Direction	Function
A[17:0]	Input	The primary 18-bit two's complement value for multiplication. The block multiplies by this value asynchronously if the optional AREG and PREG registers are omitted. When AREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
B[17:0]	Input	The second 18-bit two's complement value for multiplication if the B_INPUT attribute is set to DIRECT. The block multiplies by this value asynchronously if the optional BREG and PREG registers are omitted. When BREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
BCIN[17:0]	Input	The second 18-bit two's complement value for multiplication if the B_INPUT attribute is set to CASCADE. The block multiplies by this value asynchronously if the optional BREG and PREG registers are omitted. When BREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
P[35:0]	Output	The 36-bit two's complement product resulting from the multiplication of the two input values applied to the multiplier. If the optional AREG, BREG and PREG registers are omitted, the output operates asynchronously. Use of PREG causes this output to respond to the rising edge of CLK with the value qualified by CEP and RSTP. If PREG is omitted, but AREG and BREG are used, this output responds to the rising edge of CLK with the value qualified by CEA, RSTA, CEB, and RSTB. If PREG is omitted and only one of AREG or BREG is used, this output responds to both asynchronous and synchronous events.
BCOUT[17:0]	Output	The value being applied to the second input of the multiplier. When the optional BREG register is omitted, this output responds asynchronously in response to changes at the B[17:0] or BCIN[17:0] ports according to the setting of the B_INPUT attribute. If BREG is used, this output responds to the rising edge of CLK with the value qualified by CEB and RSTB.
CEA	Input	Clock enable qualifier for the optional AREG register. The value provided on the A[17:0] port is captured by AREG in response to a rising edge of CLK when this signal is High, provided that RSTA is Low.
RSTA	Input	Synchronous reset for the optional AREG register. AREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.
CEB	Input	Clock enable qualifier for the optional BREG register. The value provided on the B[17:0] or BCIN[17:0] port is captured by BREG in response to a rising edge of CLK when this signal is High, provided that RSTB is Low.
RSTB	Input	Synchronous reset for the optional BREG register. BREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.
CEP	Input	Clock enable qualifier for the optional PREG register. The value provided on the output of the multiplier port is captured by PREG in response to a rising edge of CLK when this signal is High, provided that RSTP is Low.
RSTP	Input	Synchronous reset for the optional PREG register. PREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.

Notes:

1. The control signals CLK, CEA, RSTA, CEB, RSTB, CEP, and RSTP have the option of inverted polarity.

Digital Clock Managers (DCMs)

Differences from the Spartan-3 Architecture

- Spartan-3E FPGAs have two, four, or eight DCMs, depending on device size.
- The variable phase shifting feature functions differently on Spartan-3E FPGAs than from Spartan-3 FPGAs.
- The Spartan-3E DLLs support lower input frequencies, down to 5 MHz. Spartan-3 DLLs support down to 18 MHz.

Overview

Spartan-3E Digital Clock Managers (DCMs) provide flexible, complete control over clock frequency, phase shift and skew. To accomplish this, the DCM employs a Delay-Locked Loop (DLL), a fully digital control system that uses feedback to maintain clock signal characteristics with a high degree of precision despite normal variations in operating temperature and voltage. This section provides a fundamental description of the DCM.

The XC3S100E FPGA has two DCMs, one at the top and one at the bottom of the device. The XC3S250E and XC3S500E FPGAs each include four DCMs, two at the top and two at the bottom. The XC3S1200E and XC3S1600E FPGAs contain eight DCMs with two on each edge (see also Figure 46). The DCM in Spartan-3E FPGAs is surrounded by CLBs within the logic array and is no longer located at the top and bottom of a column of block RAM as in the Spartan-3 architecture. The Digital Clock Manager is instantiated within a design using a “DCM” primitive.

The DCM supports three major functions:

- **Clock-skew Elimination:** Clock skew within a system occurs due to the different arrival times of a clock signal at different points on the die, typically caused by the clock signal distribution network. Clock skew increases setup and hold time requirements and increases clock-to-out times, all of which are undesirable in high frequency applications. The DCM eliminates clock skew by phase-aligning the output clock signal that it generates with the incoming clock signal. This mechanism effectively cancels out the clock distribution delays.
- **Frequency Synthesis:** The DCM can generate a wide range of different output clock frequencies derived from the incoming clock signal. This is accomplished by either multiplying and/or dividing the frequency of the input clock signal by any of several different factors.
- **Phase Shifting:** The DCM provides the ability to shift the phase of all its output clock signals with respect to the input clock signal.

Although a single design primitive, the DCM consists of four interrelated functional units: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), the Phase Shifter (PS), and the Status Logic. Each component has its associated signals, as shown in Figure 41.

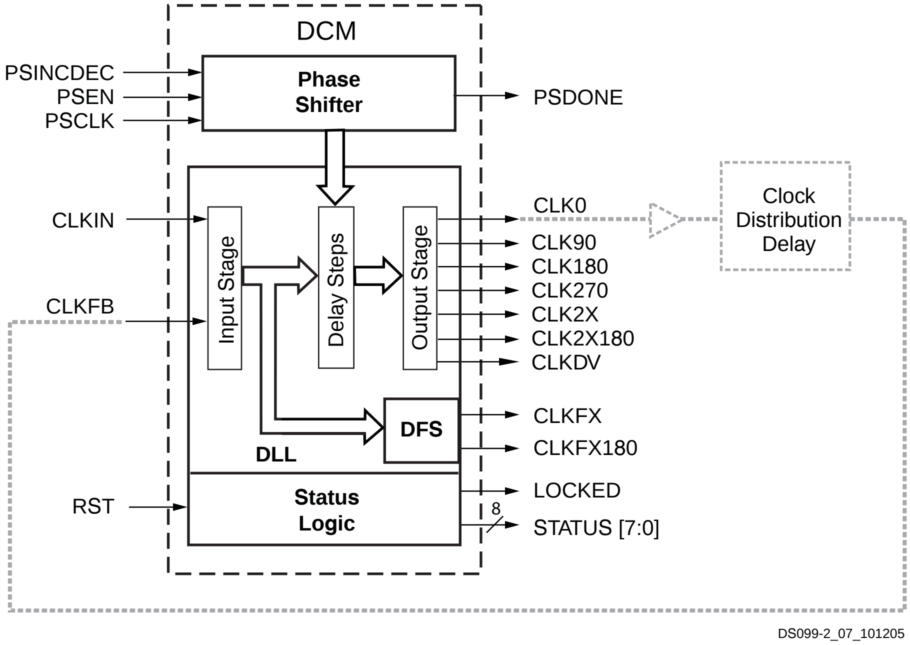


Figure 41: **DCM Functional Blocks and Associated Signals**

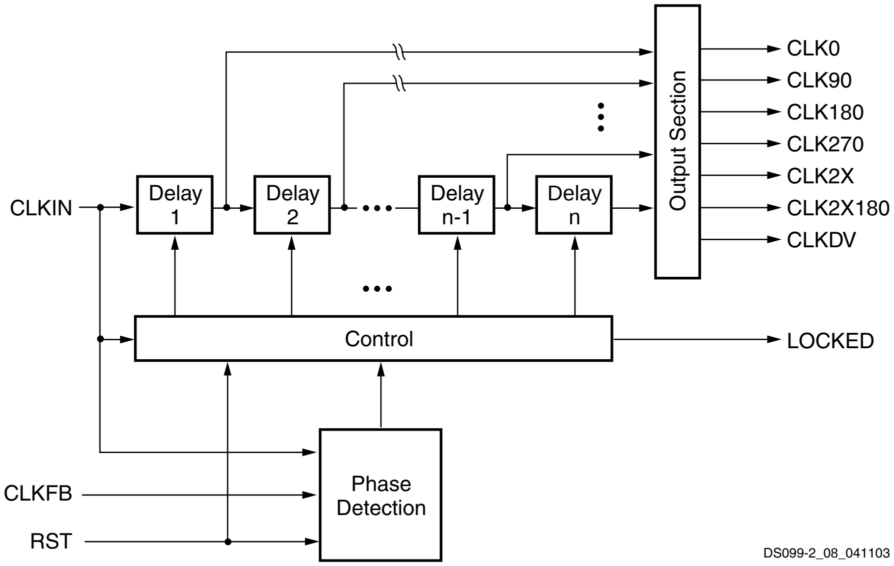


Figure 42: **Simplified Functional Diagram of DLL**

Table 28: **DLL Signals**

Signal	Direction	Description
CLKIN	Input	Receives the incoming clock signal. See Table 30, Table 31, and Table 32 for optimal external inputs to a DCM.
CLKFB	Input	Accepts either CLK0 or CLK2X as the feedback signal. (Set the CLK_FEEDBACK attribute accordingly).
CLK0	Output	Generates a clock signal with the same frequency and phase as CLKIN.
CLK90	Output	Generates a clock signal with the same frequency as CLKIN, phase-shifted by 90°.
CLK180	Output	Generates a clock signal with the same frequency as CLKIN, phase-shifted by 180°.
CLK270	Output	Generates a clock signal with the same frequency as CLKIN, phase-shifted by 270°.
CLK2X	Output	Generates a clock signal with the same phase as CLKIN, and twice the frequency.
CLK2X180	Output	Generates a clock signal with twice the frequency of CLKIN, and phase-shifted 180° with respect to CLK2X.
CLKDV	Output	Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN.

Delay-Locked Loop (DLL)

The most basic function of the DLL component is to eliminate clock skew. The main signal path of the DLL consists of an input stage, followed by a series of discrete delay elements or *steps,* which in turn leads to an output stage. This path together with logic for phase detection and control forms a system complete with feedback as shown in Figure 42. In Spartan-3E FPGAs, the DLL is implemented using a counter-based delay line.

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 28. The clock outputs drive simultaneously. Signals that initialize and report the state of the DLL are discussed in **Status Logic**.

The clock signal supplied to the CLKIN input serves as a reference waveform. The DLL seeks to align the rising-edge of feedback signal at the CLKFB input with the rising-edge of CLKIN input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network that feeds all the registers it synchronizes. These registers are either internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay steps to cancel out the clock skew. When the DLL phase-aligns the CLK0 signal with the CLKIN signal, it asserts the LOCKED output, indicating a lock on to the CLKIN signal.

DLL Attributes and Related Functions

The DLL unit has a variety of associated attributes as described in Table 29. Each attribute is described in detail in the sections that follow.

Table 29: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, ***1X***, 2X
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	***FALSE***, TRUE
CLKDV_DIVIDE	Selects the constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, ***2***, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16
CLKIN_PERIOD	Additional information that allows the DLL to operate with the most efficient lock time and the best jitter tolerance	Floating-point value representing the CLKIN period in nanoseconds

DLL Clock Input Connections

For best results, an external clock source enters the FPGA via a Global Clock Input (GCLK). Each specific DCM has four possible direct, optimal GCLK inputs that feed the DCM's CLKIN input, as shown in Table 30. Table 30 also provides the specific pin numbers by package for each GCLK input. The two additional DCM's on the XC3S1200E and XC3S1600E have similar optimal connections from the left-edge LHCLK and the right-edge RHCLK inputs, as described in Table 31 and Table 32.

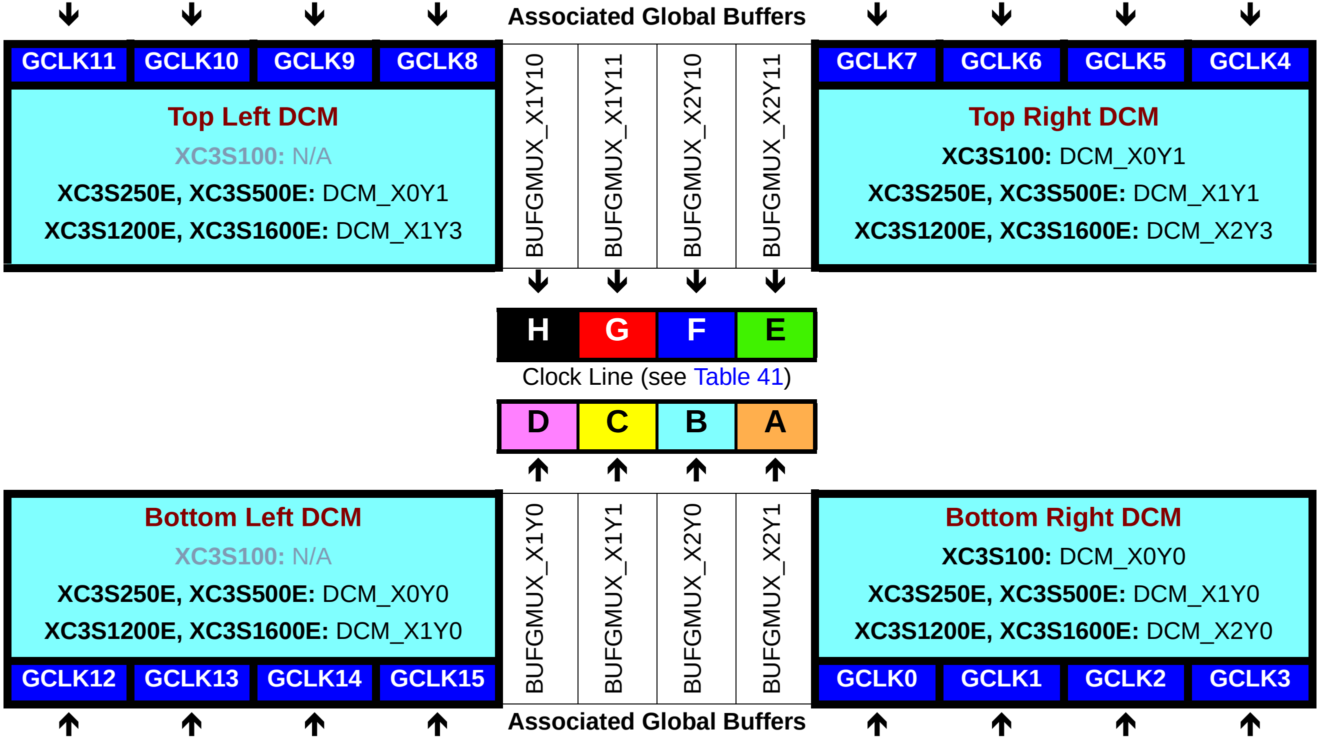
- The DCM supports differential clock inputs (for example, LVDS, LVPECL_25) via a pair of GCLK inputs that feed an internal single-ended signal to the DCM's CLKIN input.

DESIGN NOTE:

⚠ Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.

Table 30: **Direct Clock Input Connections and Optional External Feedback to Associated DCMs**

Package	Differential Pair		Differential Pair			Differential Pair		Differential Pair	
	N	P	N	P		N	P	N	P
	Pin Number for Single-Ended Input					Pin Number for Single-Ended Input			
VQ100	P91	P90	P89	P88		P86	P85	P84	P83
CP132	B7	A7	C8	B8		A9	B9	C9	A10
TQ144	P131	P130	P129	P128		P126	P125	P123	P122
PQ208	P186	P185	P184	P183		P181	P180	P178	P177
FT256	D8	C8	B8	A8		A9	A10	F9	E9
FG320	D9	C9	B9	B8		A10	B10	E10	D10
FG400	A9	A10	G10	H10		E10	E11	G11	F11
FG484	B11	C11	H11	H12		C12	B12	E12	F12



Package	Differential Pair		Differential Pair			Differential Pair		Differential Pair	
	P	N	P	N		P	N	P	N
	Pin Number for Single-Ended Input					Pin Number for Single-Ended Input			
VQ100	P32	P33	P35	P36		P38	P39	P40	P41
CP132	M4	N4	M5	N5		M6	N6	P6	P7
TQ144	P50	P51	P53	P54		P56	P57	P58	P59
PQ208	P74	P75	P77	P78		P80	P81	P82	P83
FT256	M8	L8	N8	P8		T9	R9	P9	N9
FG320	N9	M9	U9	V9		U10	T10	R10	P10
FG400	W9	W10	R10	P10		P11	P12	V10	V11
FG484	V11	U11	R11	T11		R12	P12	Y12	W12

Table 31: **Direct Clock Input and Optional External Feedback to Left-Edge DCMs (XC3S1200E and XC3S1600E)**

Diff. Clock		Single-Ended Pin Number by Package Type									Left Edge			
		VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484		LHCLK	DCM/BUFGMUX		
												BUFGMUX_X0Y5	→	D
												BUFGMUX_X0Y4	→	C
Pair	P	P9	F3	P14	P22	H5	J5	K3	M5	→	LHCLK0	DCM_X0Y2		Clock Lines
	N	P10	F2	P15	P23	H6	J4	K2	L5	→	LHCLK1			
Pair	P	P11	F1	P16	P24	H3	J1	K7	L8	→	LHCLK2			
	N	P12	G1	P17	P25	H4	J2	L7	M8	→	LHCLK3			
												BUFGMUX_X0Y3	→	B
												BUFGMUX_X0Y2	→	A
												BUFGMUX_X0Y9	→	H
												BUFGMUX_X0Y8	→	G
Pair	P	P15	G3	P20	P28	J2	K3	M1	M1	→	LHCLK4	DCM_X0Y1		Clock Lines
	N	P16	H1	P21	P29	J3	K4	L1	N1	→	LHCLK5			
Pair	P	P17	H2	P22	P30	J5	K6	M3	M3	→	LHCLK6			
	N	P18	H3	P23	P31	J4	K5	L3	M4	→	LHCLK7			
												BUFGMUX_X0Y7	→	F
												BUFGMUX_X0Y6	→	E

Table 32: **Direct Clock Input and Optional External Feedback to Right-Edge DCMs (XC3S1200E and XC3S1600E)**

		Right Edge			Single-Ended Pin Number by Package Type								Diff. Clock	
		DCM/BUFGMUX	RHCLK		VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484		
D	←	BUFGMUX_X3Y5												
C	←	BUFGMUX_X3Y4												
Clock Lines		DCM_X3Y2	RHCLK7	←	P68	G13	P94	P135	H11	J14	J20	L19	N	Pair
			RHCLK6	←	P67	G14	P93	P134	H12	J15	K20	L18	P	
			RHCLK5	←	P66	H12	P92	P133	H14	J16	K14	L21	N	Pair
			RHCLK4	←	P65	H13	P91	P132	H15	J17	K13	L20	P	
B	←	BUFGMUX_X3Y3												
A	←	BUFGMUX_X3Y2												
H	←	BUFGMUX_X3Y9												
G	←	BUFGMUX_X3Y8												
Clock Lines		DCM_X3Y1	RHCLK3	←	P63	J14	P88	P129	J13	K14	L14	M16	N	Pair
			RHCLK2	←	P62	J13	P87	P128	J14	K15	L15	M15	P	
			RHCLK1	←	P61	J12	P86	P127	J16	K12	L16	M22	N	Pair
			RHCLK0	←	P60	K14	P85	P126	K16	K13	M16	N22	P	
F	←	BUFGMUX_X3Y7												
E	←	BUFGMUX_X3Y6												

Every FPGA input provides a possible DCM clock input, but the path is not temperature and voltage compensated like the GCLKs. Alternatively, clock signals within the FPGA optionally provide a DCM clock input via a Global Clock Multiplexer Buffer (BUFGMUX). The global clock net connects directly to the CLKIN input. The internal and external connections are shown in Figure 43a and Figure 43c, respectively.

DLL Clock Output and Feedback Connections

As many as four of the nine DCM clock outputs can simultaneously drive four of the BUFGMUX buffers on the same die edge. All DCM clock outputs can simultaneously drive general routing resources, including interconnect leading to OBUF buffers.

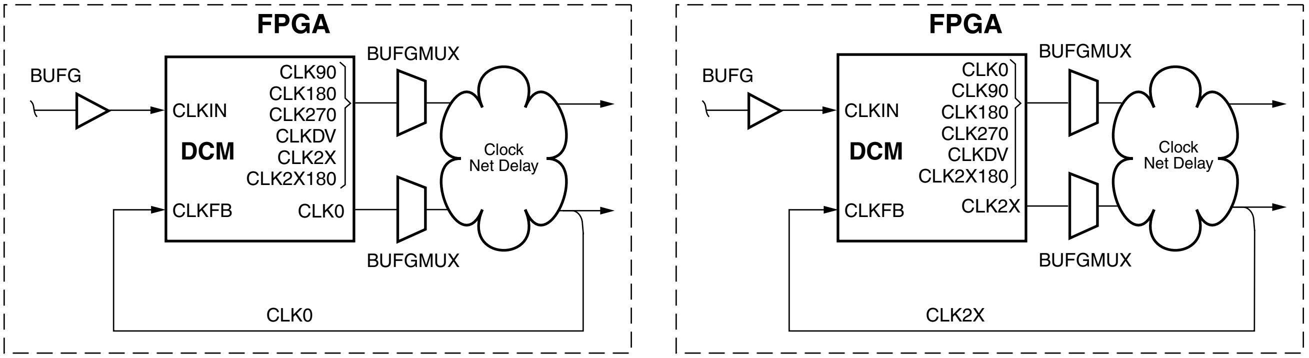
The feedback loop is essential for DLL operation. Either the CLK0 or CLK2X outputs feed back to the CLKFB input via a BUFGMUX global buffer to eliminate the clock distribution delay. The specific BUFGMUX buffer used to feed back the CLK0 or CLK2X signal is ideally one of the BUFGMUX buffers associated with a specific DCM, as shown in Table 30, Table 31, and Table 32.

The feedback path also phase-aligns the other seven DLL outputs: CLK0, CLK90, CLK180, CLK270, CLKDV, CLK2X, or CLK2X180. The CLK_FEEDBACK attribute value must agree with the physical feedback connection. Use “1X” for CLK0 feedback and “2X” for CLK2X feedback. If the DFS unit is used stand-alone, without the DLL, then no feedback is required and set the CLK_FEEDBACK attribute to “NONE”.

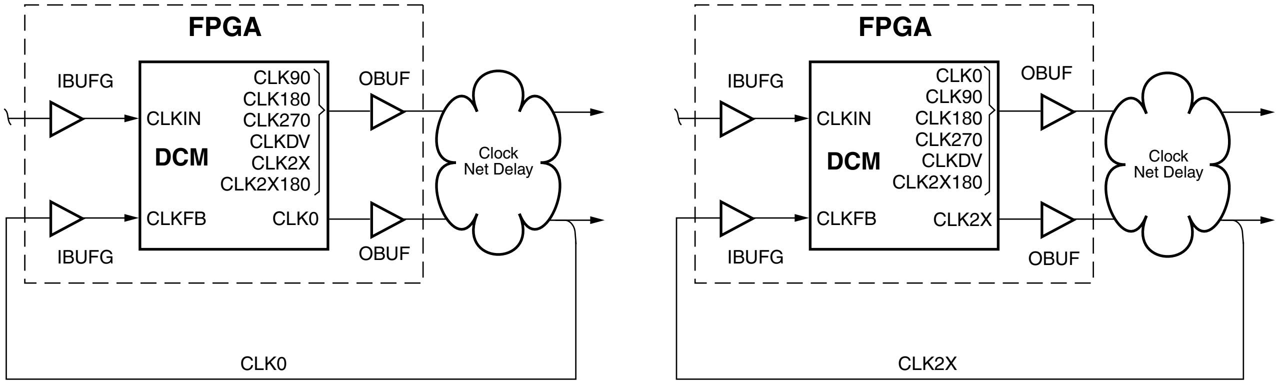
Two basic cases determine how to connect the DLL clock outputs and feedback connections: on-chip synchronization and off-chip synchronization, which are illustrated in Figure 43a through Figure 43d.

In the on-chip synchronization case in Figure 43a and Figure 43b, it is possible to connect any of the DLL’s seven output clock signals through general routing resources to the FPGA’s internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in Figure 43a, the feedback loop is created by routing CLK0 (or CLK2X) in Figure 43b to a global clock net, which in turn drives the CLKFB input.

In the off-chip synchronization case in Figure 43c and Figure 43d, CLK0 (or CLK2X) plus any of the DLL’s other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in Figure 43c, the feedback loop is formed by feeding CLK0 (or CLK2X) in Figure 43d back into the FPGA, then to the DCM’s CLKFB input via a Global Buffer Input, specified in Table 30.



(a) On-Chip with CLK0 Feedback **(b) On-Chip with CLK2X Feedback**



(c) Off-Chip with CLK0 Feedback **(d) Off-Chip with CLK2X Feedback**

Figure 43: **Input Clock, Output Clock, and Feedback Connections for the DLL**

Accommodating Input Frequencies Beyond Specified Maximums

If the CLKIN input frequency exceeds the maximum permitted, divide it down to an acceptable value using the CLKIN_DIVIDE_BY_2 attribute. When this attribute is set to "TRUE", the CLKIN frequency is divided by a factor of two as it enters the DCM. In addition, the CLKIN_DIVIDE_BY_2 option produces a 50% duty-cycle on the input clock, although at half the CLKIN frequency.

Quadrant and Half-Period Phase Shift Outputs

In addition to CLK0 for zero-phase alignment to the CLKIN signal, the DLL also provides the CLK90, CLK180, and CLK270 outputs for 90°, 180°, and 270° phase-shifted signals, respectively. These signals are described in Table 28, page 49 and their relative timing is shown in Figure 44. For control in finer increments than 90°, see **Phase Shifter (PS)**.

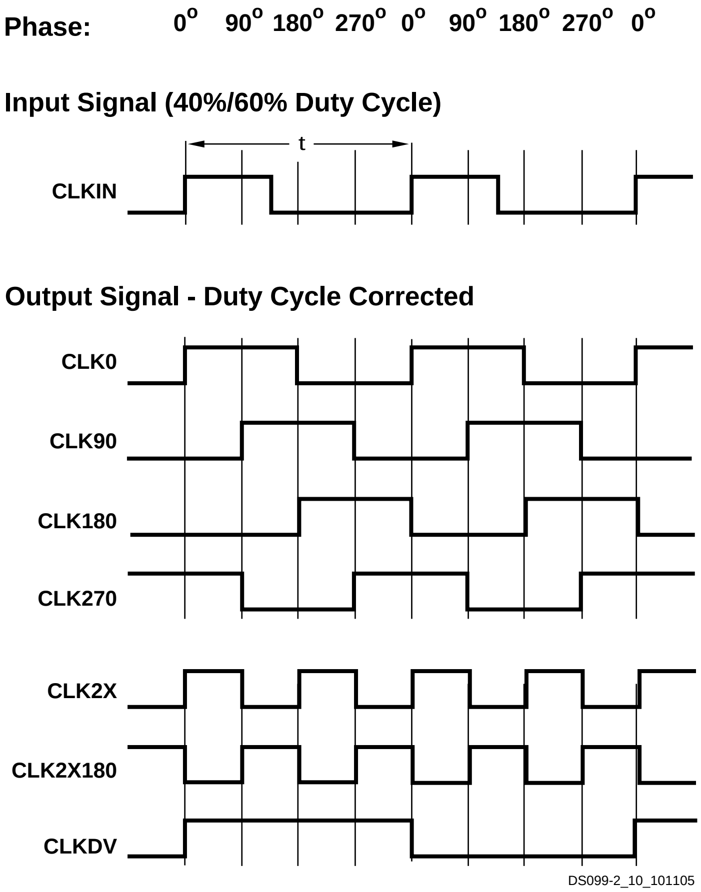


Figure 44: **Characteristics of the DLL Clock Outputs**

Basic Frequency Synthesis Outputs

The DLL component provides basic options for frequency multiplication and division in addition to the more flexible synthesis capability of the DFS component, described in a later section. These operations result in output clock signals with frequencies that are either a fraction (for division) or a multiple (for multiplication) of the incoming clock frequency. The CLK2X output produces an in-phase signal that is twice the frequency of CLKIN. The CLK2X180 output also doubles the frequency, but is 180° out-of-phase with respect to CLKIN. The CLKDIV output generates a clock frequency that is a predetermined fraction of the CLKIN frequency. The CLKDV_DIVIDE attribute determines the factor used to divide the CLKIN frequency. The attribute can be set to various values as described in Table 29. The basic frequency synthesis outputs are described in Table 28.

Duty Cycle Correction of DLL Clock Outputs

The DLL output signals exhibit a 50% duty cycle, even if the incoming CLKIN signal has a different duty cycle. Fifty-percent duty cycle means that the High and Low times of each clock cycle are equal.

DLL Performance Differences Between Steppings

As indicated in **Digital Clock Manager (DCM) Timing** (Module 3), the Stepping 1 revision silicon supports higher maximum input and output frequencies. Stepping 1 devices are backwards compatible with Stepping 0 devices.

Digital Frequency Synthesizer (DFS)

The DFS unit generates clock signals where the output frequency is a product of the CLKIN input clock frequency and a ratio of two user-specified integers. The two dedicated outputs from the DFS unit, CLKFX and CLKFX180, are defined in Table 33.

Table 33: **DFS Signals**

Signal	Direction	Description
CLKFX	Output	Multiplies the CLKIN frequency by the attribute-value ratio (CLKFX_MULTIPLY/ CLKFX_DIVIDE) to generate a clock signal with a new target frequency.
CLKFX180	Output	Generates a clock signal with the same frequency as CLKFX, but shifted 180° out-of-phase.

The signal at the CLKFX180 output is essentially an inversion of the CLKFX signal. These two outputs always exhibit a 50% duty cycle, even when the CLKIN signal does not. The DFS clock outputs are active coincident with the seven DLL outputs and their output phase is controlled by the Phase Shifter unit (PS).

The output frequency (f_{CLKFX}) of the DFS is a function of the incoming clock frequency (f_{CLKIN}) and two integer attributes, as follows.

$$f_{CLKFX} = f_{CLKIN} \bullet \left(\frac{CLKFX\_MULTIPLY}{CLKFX\_DIVIDE}\right) \qquad \text{Eq. 1}$$

The CLKFX_MULTIPLY attribute is an integer ranging from 2 to 32, inclusive, and forms the numerator in Equation 1.

The CLKFX_DIVIDE is an integer ranging from 1 to 32, inclusive and forms the denominator in Equation 1. For example, if CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, the frequency of the output clock signal is 5/3 that of the input clock signal. These attributes and their acceptable ranges are described in Table 34.

Table 34: **DFS Attributes**

Attribute	Description	Values
CLKFX_MULTIPLY	Frequency multiplier constant	Integer from 2 to 32, inclusive
CLKFX_DIVIDE	Frequency divisor constant	Integer from 1 to 32, inclusive

Any combination of integer values can be assigned to the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes, provided that two conditions are met:

1. The two values fall within their corresponding ranges, as specified in Table 34.
2. The f_{CLKFX} output frequency calculated in Equation 1 falls within the DCM's operating frequency specifications (see Table 104 in Module 3).

DFS With or Without the DLL

Although the CLKIN input is shared with both units, the DFS unit functions with or separately from the DLL unit. Separate from the DLL, the DFS generates an output frequency from the CLKIN frequency according to the respective CLKFX_MULTIPLY and CLKFX_DIVIDE values. Frequency synthesis does not require a feedback loop. Furthermore, without the DLL, the DFS unit supports a broader operating frequency range.

With the DLL, the DFS unit operates as described above, only with the additional benefit of eliminating the clock distribution delay. In this case, a feedback loop from the CLK0 or CLK2X output to the CLKFB input must be present.

When operating with the DLL unit, the DFS's CLKFX and CLKFX180 outputs are phase-aligned with the CLKIN input every CLKFX_DIVIDE cycles of CLKIN and every CLKFX_MULTIPLY cycles of CLKFX. For example, when CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, the input and output clock edges coincide every three CLKIN input periods, which is equivalent in time to five CLKFX output periods.

Smaller CLKFX_MULTIPLY and CLKFX_DIVIDE values result in faster lock times. Therefore, CLKFX_MULTIPLY and CLKFX_DIVIDE must be factored to reduce their values wherever possible. For example, given CLKFX_MULTIPLY = 9 and CLKFX_DIVIDE = 6, removing a factor of three yields CLKFX_MULTIPLY = 3 and CLKFX_DIVIDE = 2. While both value-pairs result in the multiplication of clock frequency by 3/2, the latter value-pair enables the DLL to lock more quickly.

Phase Shifter (PS)

The DCM provides two approaches to controlling the phase of a DCM clock output signal relative to the CLKIN signal: First, eight of the nine DCM clock outputs – CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, CLKFX, and CLKFX180 – provide either quadrant or half-period phase shifting of the input clock.

Second, the PS unit provides additional fine phase shift control of all nine DCM outputs. The PS unit accomplishes this by introducing a "fine phase shift" delay (T_{PS}) between the CLKFB and CLKIN signals inside the DLL unit. In FIXED phase shift mode, the fine phase shift is specified at design time with a resolution down to 1/256th of a CLKIN cycle or one delay step (DCM_DELAY_STEP), whichever is greater. This fine phase shift value is relative to the coarser quadrant or half-period phase shift of the DCM clock output. When used, the PS unit shifts the phase of all nine DCM clock output signals.

Enabling Phase Shifting and Selecting an Operating Mode

The CLKOUT_PHASE_SHIFT attribute controls the PS unit for the specific DCM instantiation. As described in Table 35, this attribute has three possible values: NONE, FIXED, and VARIABLE. When CLKOUT_PHASE_SHIFT = NONE, the PS unit is disabled and the DCM output clocks are phase-aligned to the CLKIN input via the CLKFB feedback path. Figure 45a shows this case.

The PS unit is enabled when the CLKOUT_PHASE_SHIFT attribute is set to FIXED or VARIABLE modes. These two modes are described in the sections that follow.

Table 35: **PS Attributes**

Attribute	Description	Values
CLKOUT_PHASE_SHIFT	Disables the PS component or chooses between Fixed Phase and Variable Phase modes.	***NONE***, FIXED, VARIABLE
PHASE_SHIFT	Determines size and direction of initial fine phase shift.	Integers from –255 to +255

FIXED Phase Shift Mode

The FIXED phase shift mode shifts the DCM outputs by a fixed amount (T_{PS}), controlled by the user-specified PHASE_SHIFT attribute. The PHASE_SHIFT value (shown as P in Figure 45) must be an integer ranging from –255 to +255. PHASE_SHIFT specifies a phase shift delay as a fraction of the T_{CLKIN}. The phase shift behavior is different between ISE 8.1, Service Pack 3 and prior software versions, as described below.

DESIGN NOTE:

Prior to ISE 8.1i, Service Pack 3, the FIXED phase shift feature operated differently than the Spartan-3 DCM design primitive and simulation model. Designs using software prior to ISE 8.1i, Service Pack 3 require recompilation using the latest ISE software release. Please read the following Answer Record for additional information.

Answer Record #23153

www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=23153

FIXED Phase Shift using ISE 8.1i, Service Pack 3 and later: See Equation 2. The value corresponds to a phase shift range of –360° to +360°, which matches behavior of the Spartan-3 DCM design primitive and simulation model.

$$t_{PS} = \left(\frac{\text{PHASESHIFT}}{256}\right) \bullet T_{CLKIN} \qquad \text{Eq. 2}$$

FIXED Phase Shift prior to ISE 8.1i, Service Pack 3: See Equation 3. The value corresponds to a phase shift range of –180° to +180° degrees, which is different from the Spartan-3 DCM design primitive and simulation model. Designs created prior to ISE 8.1i, Service Pack 3 must be recompiled using the most recent ISE development software.

$$t_{PS} = \left(\frac{\text{PHASESHIFT}}{512}\right) \bullet T_{CLKIN} \qquad \text{Eq. 3}$$

When the PHASE_SHIFT value is zero, CLKFB and CLKIN are in phase, the same as when the PS unit is disabled. When the PHASE_SHIFT value is positive, the DCM outputs are shifted later in time with respect to CLKIN input. When the attribute value is negative, the DCM outputs are shifted earlier in time with respect to CLKIN.

Figure 45b illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK, and PSINCDEC inputs are not used and must be tied to GND.

Equation 2 or Equation 3 applies only to FIXED phase shift mode. The VARIABLE phase shift mode operates differently.

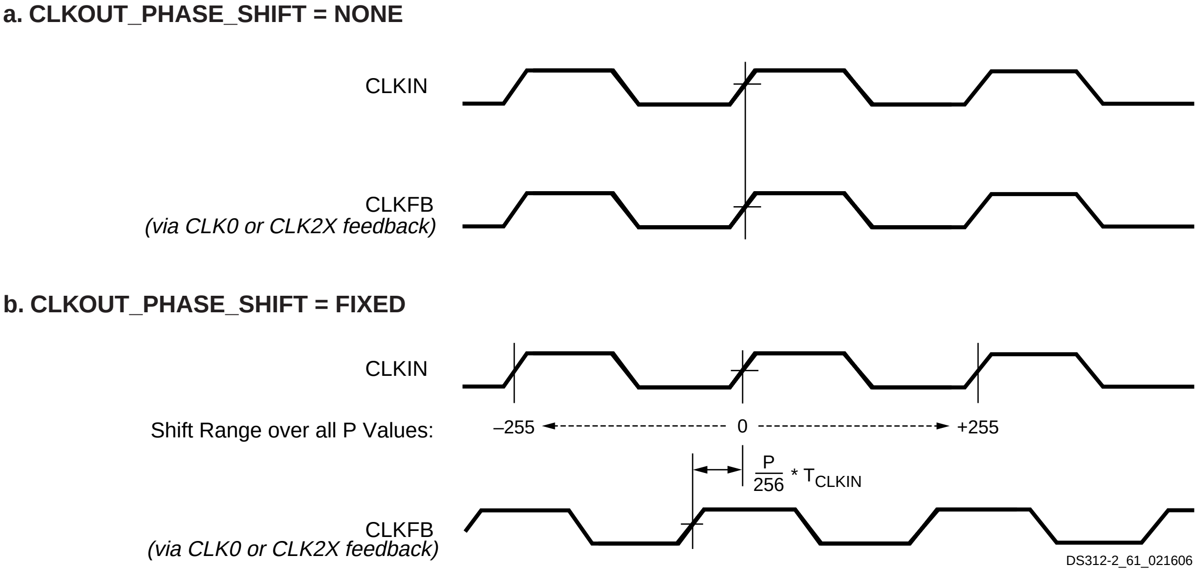


Figure 45: **NONE and FIXED Phase Shifter Waveforms (ISE 8.1i, Service Pack 3 and later)**

VARIABLE Phase Shift Mode

In VARIABLE phase shift mode, the FPGA application dynamically adjusts the fine phase shift value using three inputs to the PS unit (PSEN, PSCLK, and PSINCDEC), as defined in Table 36 and shown in Figure 41.

Table 36: **Signals for Variable Phase Mode**

Signal	Direction	Description
PSEN(1)	Input	Enables the Phase Shift unit for variable phase adjustment.
PSCLK(1)	Input	Clock to synchronize phase shift adjustment.
PSINCDEC(1)	Input	When High, increments the current phase shift value. When Low, decrements the current phase shift value. This signal is synchronized to the PSCLK signal.
PSDONE	Output	Goes High to indicate that the present phase adjustment is complete and PS unit is ready for next phase adjustment request. This signal is synchronized to the PSCLK signal.

Notes:

1. This input supports either a true or inverted polarity.

The FPGA application uses the three PS inputs on the Phase Shift unit to dynamically and incrementally increase or decrease the phase shift amount on all nine DCM clock outputs.

To adjust the current phase shift value, the PSEN enable signal must be High to enable the PS unit. Coincidently, PSINCDEC must be High to increment the current phase shift amount or Low to decrement the current amount. All VARIABLE phase shift operations are controlled by the PSCLK input, which can be the CLKIN signal or any other clock signal.

DESIGN NOTE:

The VARIABLE phase shift feature operates differently from the Spartan-3 DCM but the DCM design primitive is common to both Spartan-3 and Spartan-3E design entry. Variable phase shift in Spartan-3E FPGAs behaves as described herein. However, the DCM design primitive and simulation model does not match this behavior. Starting with ISE 8.1i, Service Pack 3, using the VARIABLE attribute generates an error message. Please read the following Answer Record to re-enable the VARIABLE phase shift feature.

Answer Record #23004
www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=23004

DCM_ DELAY_STEP is the finest delay resolution available in the PS unit. Its value is provided at the bottom of Table 102 in Module 3. For each enabled PSCLK cycle that PSINCDEC is High, the PS unit adds one DCM_ DELAY_STEP of phase shift to all nine DCM outputs. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS unit subtracts one DCM_ DELAY_STEP of phase shift from all nine DCM outputs.

Because each DCM_DELAY_STEP has a minimum and maximum value, the actual phase shift delay for the present phase increment/decrement value (VALUE) falls within the minimum and maximum values according to Equation 4 and Equation 5.

$$T_{PS}(\mathrm{Max}) = \mathrm{VALUE} \bullet \mathrm{DCM\_DELAY\_STEP\_MAX} \qquad \text{Eq. 4}$$

$$T_{PS}(\mathrm{Min}) = \mathrm{VALUE} \bullet \mathrm{DCM\_DELAY\_STEP\_MIN} \qquad \text{Eq. 5}$$

The maximum variable phase shift steps, MAX_STEPS, is described in Equation 6, for a given CLKIN input period, T_{CLKIN}, in nanoseconds. To convert this to a phase shift range measured in time and not steps, use MAX_STEPS derived in Equation 6 for VALUE in Equation 4 and Equation 5.

$$\mathrm{MAX\_STEPS} = \pm[\mathrm{INTEGER}(20 \bullet (T_{CLKIN} - 3))] \qquad \text{Eq. 6}$$

The phase adjustment might require as many as 100 CLKIN cycles plus 3 PSCLK cycles to take effect, at which point the DCM's PSDONE output goes High for one PSCLK cycle. This pulse indicates that the PS unit completed the previous adjustment and is now ready for the next request.

Asserting the Reset (RST) input returns the phase shift to zero.

Status Logic

The Status Logic indicates the present state of the DCM and a means to reset the DCM to its initial known state. The Status Logic signals are described in Table 37.

In general, the Reset (RST) input is only asserted upon configuring the FPGA or when changing the CLKIN frequency. The RST signal must be asserted for three or more CLKIN cycles. A DCM reset does not affect attribute values (for example, CLKFX_MULTIPLY and CLKFX_DIVIDE). If not used, RST is tied to GND.

The eight bits of the STATUS bus are described in Table 38.

Table 37: **Status Logic Signals**

Signal	Direction	Description
RST	Input	A High resets the entire DCM to its initial power-on state. Initializes the DLL taps for a delay of zero. Sets the LOCKED output Low. This input is asynchronous.
STATUS[7:0]	Output	The bit values on the STATUS bus provide information regarding the state of DLL and PS operation
LOCKED	Output	Indicates that the CLKIN and CLKFB signals are in phase by going High. The two signals are out-of-phase when Low.

Table 38: **DCM Status Bus**

Bit	Name	Description
0	Reserved	-
1	CLKIN Stopped	When High, indicates that the CLKIN input signal is not toggling. When Low, indicates CLKIN is toggling. This bit functions only when the CLKFB input is connected.(1)
2	CLKFX Stopped	When High, indicates that the CLKFX output is not toggling. When Low, indicates the CLKFX output is toggling. This bit functions only when the CLKFX or CLKFX180 output are connected.
3-6	Reserved	-

Notes:

1. When only the DFS clock outputs but none of the DLL clock outputs are used, this bit does not go High when the CLKIN signal stops.

Stabilizing DCM Clocks Before User Mode

The STARTUP_WAIT attribute shown in Table 39 optionally delays the end of the FPGA's configuration process until after the DCM locks to its incoming clock frequency. This option ensures that the FPGA remains in the Startup phase of configuration until all clock outputs generated by the DCM are stable. When all DCMs that have their STARTUP_WAIT attribute set to TRUE assert the LOCKED signal, then the FPGA completes its configuration process and proceeds to user mode. The associated bitstream generator (BitGen) option ***LCK_cycle*** specifies one of the six cycles in the Startup phase. The selected cycle defines the point at which configuration stalls until all the LOCKED outputs go High. See **Start-Up**, page 107 for more information.

Table 39: **STARTUP_WAIT Attribute**

Attribute	Description	Values
STARTUP_WAIT	When TRUE, delays transition from configuration to user mode until DCM locks to the input clock.	TRUE, ***FALSE***

Clocking Infrastructure

The Spartan-3E clocking infrastructure, shown in Figure 46, provides a series of low-capacitance, low-skew interconnect lines well-suited to carrying high-frequency signals throughout the FPGA. The infrastructure also includes the clock inputs and BUFGMUX clock buffers/multiplexers. The Xilinx Place-and-Route (PAR) software automatically routes high-fanout clock signals using these resources.

Clock Inputs

Clock pins accept external clock signals and connect directly to DCMs and BUFGMUX elements. Each Spartan-3E FPGA has:

- 16 Global Clock inputs (GCLK0 through GCLK15) located along the top and bottom edges of the FPGA
- 8 Right-Half Clock inputs (RHCLK0 through RHCLK7) located along the right edge
- 8 Left-Half Clock inputs (LHCLK0 through LHCLK7) located along the left edge

DESIGN NOTE:

Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.

Clock inputs optionally connect directly to DCMs using dedicated connections. Table 30, Table 31, and Table 32 show the clock inputs that best feed a specific DCM within a given Spartan-3E part number. Different Spartan-3E FPGA densities have different numbers of DCMs. The XC3S1200E and XC3S1600E are the only two densities with the left- and right-edge DCMs.

Each clock input is also optionally a user-I/O pin and connects to internal interconnect. Some clock pad pins are input-only pins as indicated in **Pinout Descriptions** (Module 4).

Clock Buffers/Multiplexers

Clock Buffers/Multiplexers either drive clock input signals directly onto a clock line (BUFG) or optionally provide a multiplexer to switch between two unrelated, possibly asynchronous clock signals (BUFGMUX).

Each BUFGMUX element, shown in Figure 47, is a 2-to-1 multiplexer. The select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX's output signal, O, as described in Table 40. The switching from one clock to the other is glitch-less, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock. As specified in **DC and Switching Characteristics** (Module 3), the select input has a setup time requirement.

Table 40: **BUFGMUX Select Mechanism**

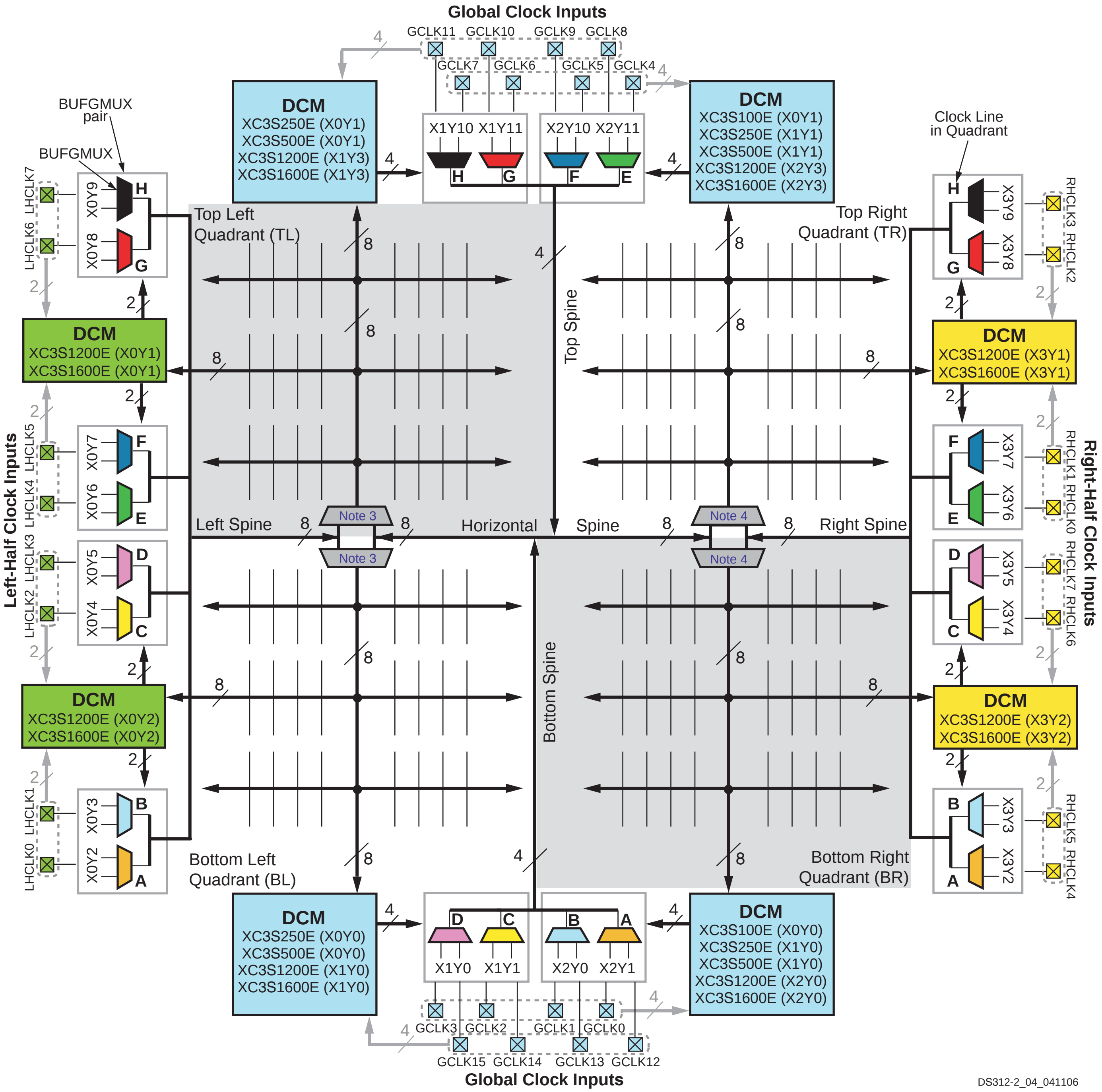
S Input	O Output
0	I0 Input
1	I1 Input

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

The I0 and I1 inputs to an BUFGMUX element originate from clock input pins, DCMs, or Double-Line interconnect, as shown in Figure 47. As shown in Figure 46, there are 24 BUFGMUX elements distributed around the four edges of the device. Clock signals from the four BUFGMUX elements at the top edge and the four at the bottom edge are truly global and connect to all clocking quadrants. The eight left-edge BUFGMUX elements only connect to the two clock quadrants in the left half of the device. Similarly, the eight right-edge BUFGMUX elements only connect to the right half of the device.

BUFGMUX elements are organized in pairs and share I0 and I1 connections with adjacent BUFGMUX elements from a common clock switch matrix as shown in Figure 47. For example, the input on I0 of one BUFGMUX is also a shared input to I1 of the adjacent BUFGMUX.

The clock switch matrix for the left- and right-edge BUFGMUX elements receive signals from any of the three following sources: an LHCLK or RHCLK pin as appropriate, a Double-Line interconnect, or a DCM in the XC3S1200E and XC3S1600E devices.



Notes:

1. The diagram presents electrical connectivity. The diagram locations do not necessarily match the physical location on the device, although the coordinate locations shown are correct.
2. Number of DCMs and locations of these DCM varies for different device densities. The left and right DCMs are only in the XC3S1200E and XC3S1600E. The XC3S100E has only two DCMs, one on the top right and one on the bottom right of the die.
3. See Figure 48a, which shows how the eight clock lines are multiplexed on the left-hand side of the device.
4. See Figure 48b, which shows how the eight clock lines are multiplexed on the right-hand side of the device.
5. For best direct clock inputs to a particular clock buffer, not a DCM, see Table 41.
6. For best direct clock inputs to a particular DCM, not a BUFGMUX, see Table 30, Table 31, and Table 32. Direct pin inputs to a DCM are shown in gray.

Figure 46: **Spartan-3E Internal Quadrant-Based Clock Network (Electrical Connectivity View)**

By contrast, the clock switch matrixes on the top and bottom edges receive signals from any of the five following sources: two GCLK pins, two DCM outputs, or one Double-Line interconnect.

Table 41 indicates permissible connections between clock inputs and BUFGMUX elements. The I0-input provides the best input path to a clock buffer. The I1-input provides the secondard input for the clock multiplexer function.

The four BUFGMUX elements on the top edge are paired together and share inputs from the eight global clock inputs along the top edge. Each BUFGMUX pair connects to four of the eight global clock inputs, as shown in Figure 46. This optionally allows differential inputs to the global clock inputs without wasting a BUFGMUX element.

Table 41: **Connections from Clock Inputs to BUFGMUX Elements and Associated Quadrant Clock**

Quadrant Clock Line(1)	**Left-Half BUFGMUX**			**Top or Bottom BUFGMUX**			**Right-Half BUFGMUX**		
	Location(2)	**I0 Input**	**I1 Input**	**Location(2)**	**I0 Input**	**I1 Input**	**Location(2)**	**I0 Input**	**I1 Input**
H	*X0Y9*	LHCLK7	LHCLK6	*X1Y10*	GCLK7 or GCLK11	GCLK6 or GCLK10	*X3Y9*	RHCLK3	RHCLK2
G	*X0Y8*	LHCLK6	LHCLK7	*X1Y11*	GCLK6 or GCLK10	GCLK7 or GCLK11	*X3Y8*	RHCLK2	RHCLK3
F	*X0Y7*	LHCLK5	LHCLK4	*X2Y10*	GCLK5 or GCLK9	GCLK4 or GCLK8	*X3Y7*	RHCLK1	RHCLK0
E	*X0Y6*	LHCLK4	LHCLK5	*X2Y11*	GCLK4 or GCLK8	GCLK5 or GCLK9	*X3Y6*	RHCLK0	RHCLK1
D	*X0Y5*	LHCLK3	LHCLK2	*X1Y0*	GCLK3 or GCLK15	GCLK2 or GCLK14	*X3Y5*	RHCLK7	RHCLK6
C	*X0Y4*	LHCLK2	LHCLK3	*X1Y1*	GCLK2 or GCLK14	GCLK3 or GCLK15	*X3Y4*	RHCLK6	RHCLK7
B	*X0Y3*	LHCLK1	LHCLK0	*X2Y0*	GCLK1 or GCLK13	GCLK0 or GCLK12	*X3Y3*	RHCLK5	RHCLK4
A	*X0Y2*	LHCLK0	LHCLK1	*X2Y1*	GCLK0 or GCLK12	GCLK1 or GCLK13	*X3Y2*	RHCLK4	RHCLK5

Notes:

1. See **Quadrant Clock Routing** for connectivity details for the eight quadrant clocks.
2. See Figure 46 for specific BUFGMUX locations, and Figure 48 for information on how BUFGMUX elements drive onto a specific clock line within a quadrant.

The connections for the bottom-edge BUFGMUX elements are similar to the top-edge connections (see Figure 47).

On the left and right edges, only two clock inputs feed each pair of BUFGMUX elements.

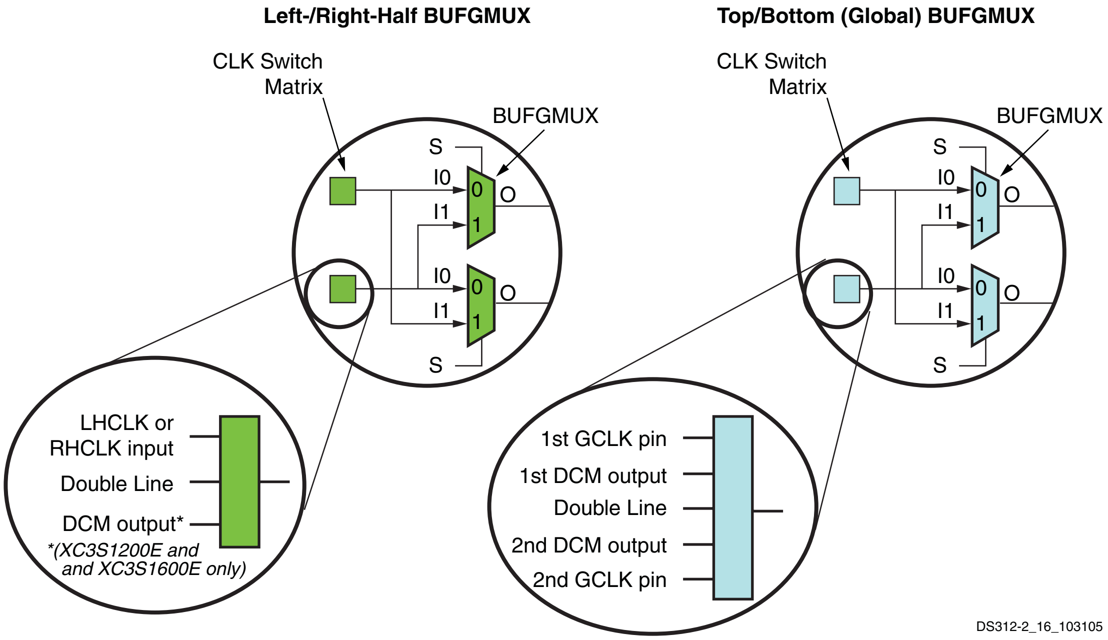


Figure 47: **Clock Switch Matrix to BUFGMUX Pair Connectivity**

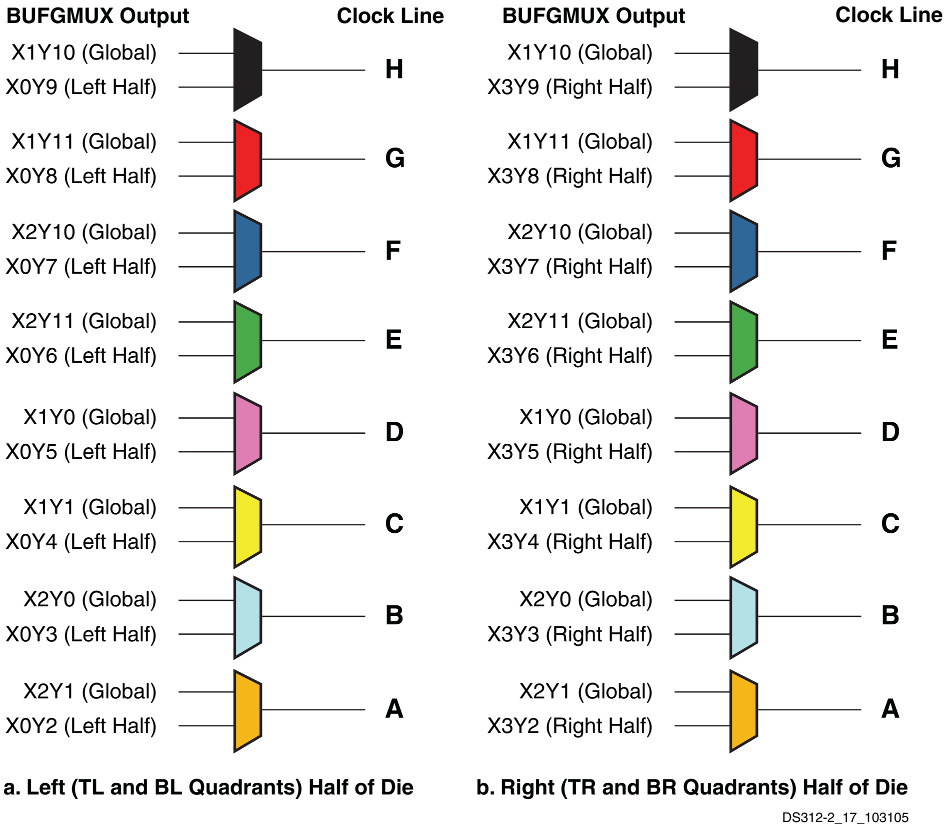
Quadrant Clock Routing

The clock routing within the FPGA is quadrant-based, as shown in Figure 46. Each clock quadrant supports eight total clock signals, labeled ‘A’ through ‘H’ in Table 41 and Figure 48. The clock source for an individual clock line originates either from a global BUFGMUX element along the top and bottom edges or from a BUFGMUX element along the associated edge, as shown in Figure 48. The clock lines feed the synchronous resource elements (CLBs, IOBs, block RAM, multipliers, and DCMs) within the quadrant.

The four quadrants of the device are:

- Top Right (TR)
- Bottom Right (BR)
- Bottom Left (BL)
- Top Left (TL)

Note that the quadrant clock notation (TR, BR, BL, TL) is separate from that used for similar IOB placement constraints.



a. Left (TL and BL Quadrants) Half of Die

b. Right (TR and BR Quadrants) Half of Die

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Figure 48: **Clock Sources for the Eight Clock Lines within a Clock Quadrant**

The outputs of the top or bottom BUFGMUX elements connect to two vertical spines, each comprising four vertical clock lines as shown in Figure 46. At the center of the die, these clock signals connect to the eight-line horizontal clock spine.

Outputs of the left and right BUFGMUX elements are routed onto the left or right horizontal spines, each comprising eight horizontal clock lines.

Each of the eight clock signals in a clock quadrant derives either from a global clock signal or a half clock signal. In other words, there are up to 24 total potential clock inputs to the FPGA, eight of which can connect to clocked elements in a single clock quadrant. Figure 48 shows how the clock lines in each quadrant are selected from associated BUFGMUX sources. For example, if quadrant clock 'A' in the bottom left (BL) quadrant originates from BUFGMUX_X2Y1, then the clock signal from BUFGMUX_X0Y2 is unavailable in the bottom left quadrant. However, the top left (TL) quadrant clock 'A' can still solely use the output from either BUFGMUX_X2Y1 or BUFGMUX_X0Y2 as the source.

To minimize the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock segments not in use.

Performance Differences between Top/Bottom and Left-/Right-Half Global Buffers

The top and bottom global buffers support higher clock frequencies than the left- and right-half buffers. Consequently, clocks exceeding 230 MHz must use the top or bottom global buffers and, if required for the application, their associated DCMs. See Table 98 in Module 3.

Interconnect

Interconnect is the programmable network of signal pathways between the inputs and outputs of functional elements within the FPGA, such as IOBs, CLBs, DCMs, and block RAM.

Interconnect, also called routing, is segmented for optimal connectivity. Functionally, interconnect resources are identical to that of the Spartan-3 architecture. There are four kinds of interconnects: long lines, hex lines, double lines, and direct lines. The Xilinx Place and Route (PAR) software exploits the rich interconnect array to deliver optimal system performance and the fastest compile times.

The switch matrix connects to the different kinds of interconnects across the device. An interconnect tile, shown in Figure 49, is defined as a single switch matrix connected to a functional element, such as a CLB, IOB, or DCM. If a functional element spans across multiple switch matrices such as the block RAM or multipliers, then an interconnect tile is defined by the number of switch matrices connected to that functional element. A Spartan-3E device can be represented as an array of interconnect tiles where interconnect resources are for the channel between any two adjacent interconnect tile rows or columns as shown in Figure 50.

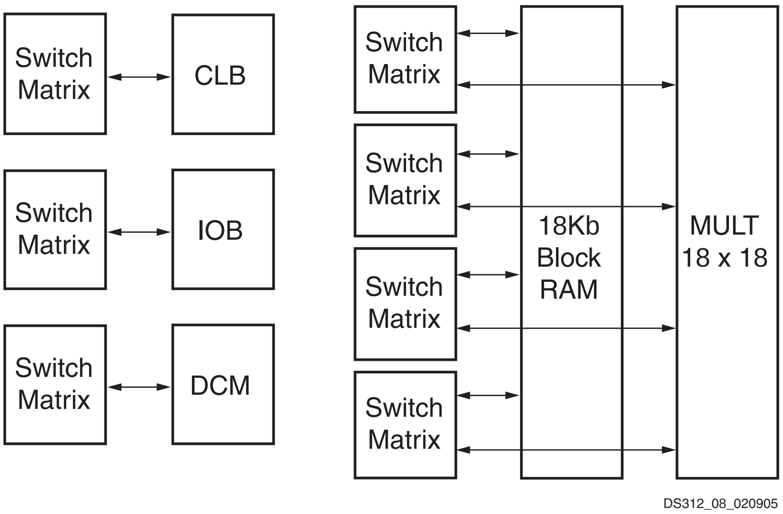


Figure 49: **Four Types of Interconnect Tiles (CLBs, IOBs, DCMs, and Block RAM/Multiplier)**

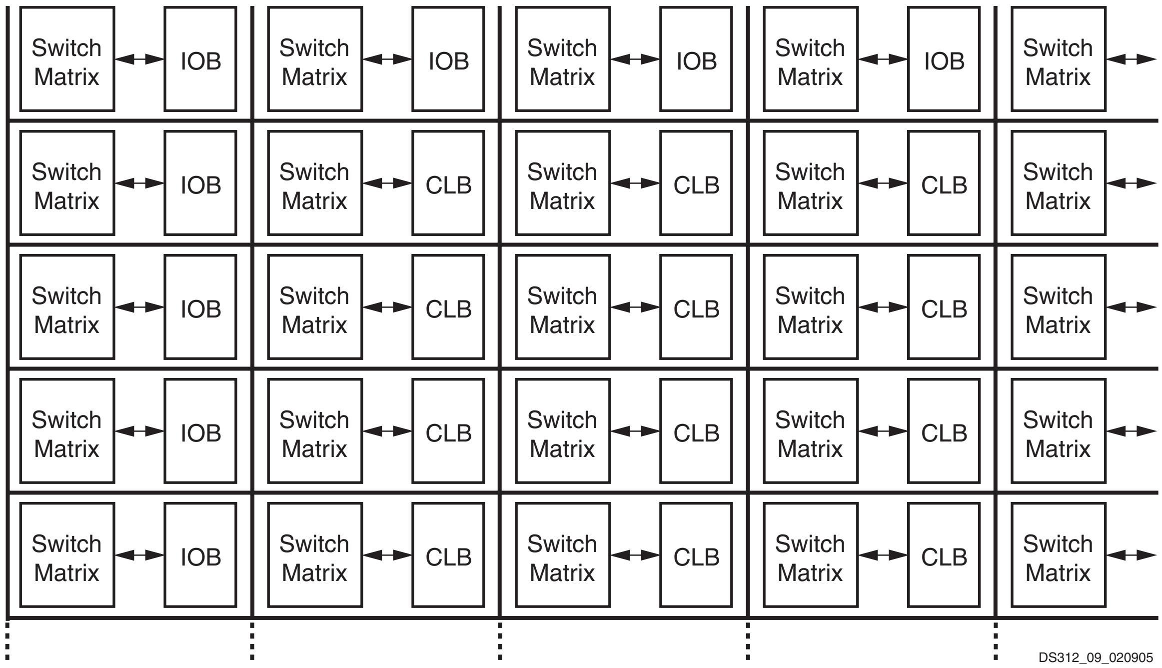
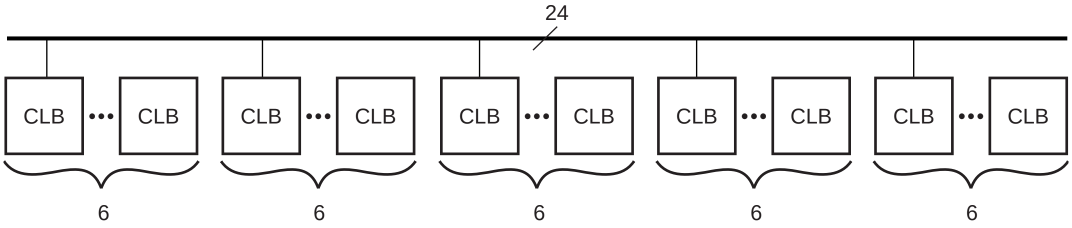
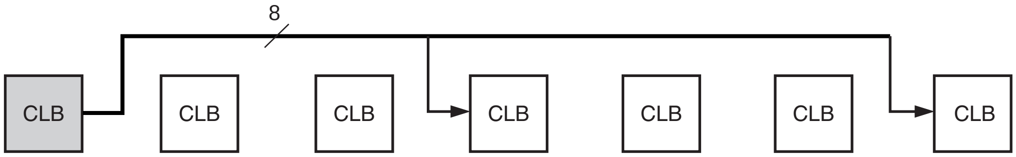
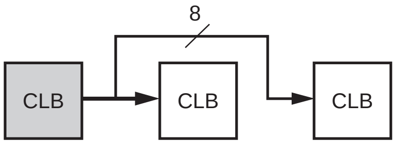
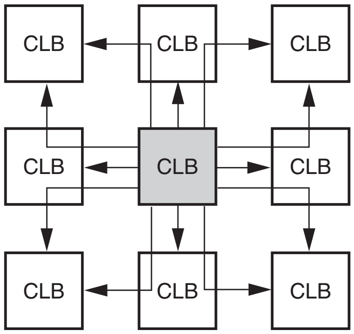


Figure 50: **Array of Interconnect Tiles in Spartan-3E FPGA**

<table>
<tr><td>Horizontal and Vertical Long Lines
(horizontal channel shown as an example)</td><td>


DS312-2_10_022305
</td></tr>
<tr><td>Horizontal and Vertical Hex Lines
(horizontal channel shown as an example)</td><td>


DS312-2_11_020905
</td></tr>
<tr><td>Horizontal and Vertical Double Lines
(horizontal channel shown as an example)</td><td>


DS312-2_15_022305
</td></tr>
<tr><td>Direct Connections</td><td>


DS312-2_12_020905
</td></tr>
</table>

Figure 51: **Interconnect Types between Two Adjacent Interconnect Tiles**

The four types of general-purpose interconnect available in each channel, shown in Figure 51, are described below.

Long Lines

Each set of 24 long line signals spans the die both horizontally and vertically and connects to one out of every six interconnect tiles. At any tile, four of the long lines drive or receive signals from a switch matrix. Because of their low capacitance, these lines are well-suited for carrying high-frequency signals with minimal loading effects (e.g. skew). If all global clock lines are already committed and additional clock signals remain to be assigned, long lines serve as a good alternative.

Hex Lines

Each set of eight hex lines are connected to one out of every three tiles, both horizontally and vertically. Thirty-two hex lines are available between any given interconnect tile. Hex lines are only driven from one end of the route.

Double Lines

Each set of eight double lines are connected to every other tile, both horizontally and vertically. in all four directions. Thirty-two double lines available between any given interconnect tile. Double lines are more connections and more flexibility, compared to long line and hex lines.

Direct Connections

Direct connect lines route signals to neighboring tiles: vertically, horizontally, and diagonally. These lines most often drive a signal from a "source" tile to a double, hex, or long line and conversely from the longer interconnect back to a direct line accessing a "destination" tile.

Global Controls (STARTUP_SPARTAN3E)

In addition to the general-purpose interconnect, Spartan-3E FPGAs have two global logic control signals, as described in Table 42. These signals are available to the FPGA application via the STARTUP_SPARTAN3E primitive.

Table 42: **Spartan-3E Global Logic Control Signals**

Global Control Input	Description
GSR	**Global Set/Reset:** When High, asynchronously places all registers and flip-flops in their initial state (see **Initialization**, page 32). Asserted automatically during the FPGA configuration process (see **Start-Up**, page 107).
GTS	**Global Three-State:** When High, asynchronously forces all I/O pins to a high-impedance state (Hi-Z, three-state).

The Global Set/Reset (GSR) signal replaces the global reset signal included in many ASIC-style designs. Use the GSR control instead of a separate global reset signal in the design to free up CLB inputs, resulting in a smaller, more efficient design. Similarly, the GSR signal is asserted automatically during the FPGA configuration process, guaranteeing that the FPGA starts-up in a known state.

The STARTUP_SPARTAN3E primitive also includes two other signals used specifically during configuration. The MBT signals are for **Dynamically Loading Multiple Configuration Images Using MultiBoot Option**, page 93. The CLK input is an alternate clock for configuration **Start-Up**, page 107.

Configuration

Differences from Spartan-3 FPGAs

In general, Spartan-3E FPGA configuration modes are a superset to those available in Spartan-3 FPGAs. Two new modes added in Spartan-3E FPGAs provide a glue-less configuration interface to industry-standard parallel NOR Flash and SPI serial Flash memories. Unlike Spartan-3 FPGAs, nearly all of the Spartan-3E configuration pins become available as user I/Os after configuration.

Configuration Process

The function of a Spartan-3E FPGA is defined by loading application-specific configuration data into the FPGA's internal, reprogrammable CMOS configuration latches (CCLs), similar to the way a microprocessor's function is defined by its application program. For FPGAs, this configuration process uses a subset of the device pins, some of which are dedicated to configuration; other pins are merely borrowed and returned to the application as general-purpose user I/Os after configuration completes.

Spartan-3E FPGAs offer several configuration options to minimize the impact of configuration on the overall system design. In some configuration modes, the FPGA generates a clock and loads itself from an external memory source, either serially or via a byte-wide data path. Alternatively, an external host such as a microprocessor downloads the FPGA's configuration data using a simple synchronous serial interface or via a byte-wide peripheral-style interface. Furthermore, multiple-FPGA designs share a single configuration memory source, creating a structure called a daisy chain.

Three FPGA pins—M2, M1, and M0—select the desired configuration mode. The mode pin settings appear in Table 43. The mode pin values are sampled during the start of configuration when the FPGA's INIT_B output goes High. After the FPGA completes configuration, the mode pins are available as user I/Os.

Table 43: **Spartan-3E Configuration Mode Options and Pin Settings**

	Master Serial	SPI	BPI	Slave Parallel	Slave Serial	JTAG
M[2:0] mode pin settings	<0:0:0>	<0:0:1>	<0:1:0>=Up <0:1:1>=Down	<1:1:0>	<1:1:1>	<1:0:1>
Data width	Serial	Serial	Byte-wide	Byte-wide	Serial	Serial
Configuration memory source	Xilinx Platform Flash	Industry-standard SPI serial Flash	Industry-standard parallel NOR Flash or Xilinx parallel Platform Flash	Any source via microcontroller, CPU, Xilinx parallel Platform Flash, etc.	Any source via microcontroller, CPU, Xilinx Platform Flash, etc.	Any source via microcontroller, CPU, System ACE™ CF, etc.
Clock source	Internal oscillator	Internal oscillator	Internal oscillator	External clock on CCLK pin	External clock on CCLK pin	External clock on TCK pin
Total I/O pins borrowed during configuration	8	13	46	21	8	0
Configuration mode for downstream daisy-chained FPGAs	Slave Serial	Slave Serial	Slave Parallel	Slave Parallel or Memory Mapped	Slave Serial	JTAG
Stand-alone FPGA applications (no external download host)	✓	✓	✓	Possible using XCFxxP Platform Flash, which optionally generates CCLK	Possible using XCFxxP Platform Flash, which optionally generates CCLK	
Uses low-cost, industry-standard Flash		✓	✓			
Supports optional MultiBoot, multi-configuration mode			✓			

Configuration Bitstream Image Sizes

A specific Spartan-3E part type always requires a constant number of configuration bits, regardless of design complexity, as shown in Table 44. The configuration file size for a multiple-FPGA daisy-chain design roughly equals the sum of the individual file sizes.

Table 44: **Number of Bits to Program a Spartan-3E FPGA (Uncompressed Bitstreams)**

Spartan-3E FPGA	Number of Configuration Bits
XC3S100E	581,344
XC3S250E	1,353,728
XC3S500E	2,270,208
XC3S1200E	3,841,184
XC3S1600E	5,969,696

Pin Behavior During Configuration

Table 45 shows how various pins behave during the FPGA configuration process. The actual behavior depends on the values applied to the M2, M1, and M0 mode select pins and the HSWAP pin. The mode select pins determine which of the I/O pins are borrowed during configuration and how they function. In JTAG configuration mode, no user-I/O pins are borrowed for configuration.

All user-I/O pins, input-only pins, and dual-purpose pins that are not actively involved in the currently-select configuration mode are high impedance (floating, three-stated, Hi-Z) during the configuration process. These pins are indicated in Table 45 as gray shaded table entries or cells.

The HSWAP input controls whether all user-I/O pins, input-only pins, and dual-purpose pins have a pull-up resistor to the supply rail or not. When HSWAP is Low, each pin has an internal pull-up resistor that is active throughout configuration. After configuration, pull-up and pull-down resistors are available in the FPGA application as described in **Pull-Up and Pull-Down Resistors**.

The yellow-shaded table entries or cells represent pins where the pull-up resistor is always enabled during configuration, regardless of the HSWAP input. The post-configuration behavior of these pins is defined by Bitstream Generator options as defined in Table 68.

Table 45: **Pin Behavior during Configuration**

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	Supply/ I/O Bank
IO* (user-I/O) IP* (input-only)							-
TDI	TDI	TDI	TDI	TDI	TDI	TDI	V_{CCAUX}
TMS	TMS	TMS	TMS	TMS	TMS	TMS	V_{CCAUX}
TCK	TCK	TCK	TCK	TCK	TCK	TCK	V_{CCAUX}
TDO	TDO	TDO	TDO	TDO	TDO	TDO	V_{CCAUX}
PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	V_{CCAUX}
DONE	DONE	DONE	DONE	DONE	DONE	DONE	V_{CCAUX}
HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	0
M2	0	0	0	1	1	1	2
M1	0	0	1	0	1	1	2
M0	0	1	0 = Up 1 = Down	1	0	1	2
CCLK	CCLK (I/O)	CCLK (I/O)	CCLK (I/O)		CCLK (I)	CCLK (I)	2
INIT_B	INIT_B	INIT_B	INIT_B		INIT_B	INIT_B	2
CSO_B		CSO_B	CSO_B		CSO_B		2
DOUT/BUSY	DOUT	DOUT	BUSY		BUSY	DOUT	2
MOSI/CSI_B		MOSI	CSI_B		CSI_B		2
D7			D7		D7		2
D6			D6		D6		2
D5			D5		D5		2
D4			D4		D4		2

Table 45: **Pin Behavior during Configuration *(Continued)***

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	Supply/ I/O Bank
D3			D3		D3		2
D2			D2		D2		2
D1			D1		D1		2
D0/DIN	DIN	DIN	D0		D0	DIN	2
RDWR_B			RDWR_B		RDWR_B		2
A23			A23				2
A22			A22				2
A21			A21				2
A20			A20				2
A19/VS2		VS2	A19				2
A18/VS1		VS1	A18				2
A17/VS0		VS0	A17				2
A16			A16				1
A15			A15				1
A14			A14				1
A13			A13				1
A12			A12				1
A11			A11				1
A10			A10				1
A9			A9				1
A8			A8				1
A7			A7				1
A6			A6				1
A5			A5				1
A4			A4				1
A3			A3				1
A2			A2				1
A1			A1				1
A0			A0				1
LDC0			LDC0				1
LDC1			LDC1				1
LDC2			LDC2				1
HDC			HDC				1

Notes:

1. Gray shaded cells represent pins that are in a high-impedance state (Hi-Z, floating) during configuration. These pins have an optional internal pull-up resistor to their respective V_{CCO} supply pin that is active throughout configuration if the HSWAP input is Low.
2. Yellow shaded cells represent pins with an internal pull-up resistor to its respective voltage supply rail that is active during configuration, regardless of the HSWAP pin.

The HSWAP pin itself has an pull-up resistor enabled during configuration. However, the VCCO_0 supply voltage must be applied before the pull-up resistor becomes active. If the VCCO_0 supply ramps after the VCCO_2 power supply, do not let HSWAP float; tie HSWAP to the desired logic level externally.

Spartan-3E FPGAs have only six dedicated configuration pins, including the DONE and PROG_B pins, and the four JTAG boundary-scan pins: TDI, TDO, TMS, and TCK. All other configuration pins are dual-purpose I/O pins and are available to the FPGA application after the DONE pin goes High. See **Start-Up** for additional information.

Table 46: **Default I/O Standard Setting During Configuration (VCCO_2 = 2.5V)**

Pin(s)	I/O Standard	Output Drive	Slew Rate
All, including CCLK	LVCMOS25	8 mA	Slow

Table 46 shows the default I/O standard setting for the various configuration pins during the configuration process. The configuration interface is designed primarily for 2.5V operation when the VCCO_2 (and VCCO_1 in BPI mode) connects to 2.5V.

The configuration pins also operate at other voltages by setting VCCO_2 (and VCCO_1 in BPI mode) to either 3.3V or 1.8V. The change on the V_{CCO} supply also changes the I/O drive characteristics. For example, with V_{CCO} = 3.3V, the output current when driving High, I_{OH}, increases to approximately 12 to 16 mA, while the current when driving Low, I_{OL}, remains 8 mA. At V_{CCO} = 1.8V, the output current when driving High, I_{OH}, decreases slightly to approximately 6 to 8 mA. Again, the current when driving Low, I_{OL}, remains 8 mA.

CCLK Design Considerations

The FPGA's configuration process is controlled by the CCLK configuration clock. Consequently, signal integrity of CCLK is important to guarantee successful configuration. Poor CCLK signal integrity caused by ringing or reflections might cause double-clocking, causing the configuration process to fail.

Although the CCLK frequency is relatively low, Spartan-3E FPGA output edge rates are fast. Therefore, careful attention must be paid to the CCLK signal integrity on the printed circuit board. Signal integrity simulation with IBIS is recommended. For all configuration modes except JTAG, the signal integrity must be considered at every CCLK trace destination, including the FPGA's CCLK pin.

This analysis is especially important when the FPGA re-uses the CCLK pin as a user-I/O after configuration. In these cases, there might be unrelated devices attached to CCLK, which add additional trace length and signal destinations.

In the Master Serial, SPI, and BPI configuration modes, the FPGA drives the CCLK pin and CCLK should be treated as a full bidirectional I/O pin for signal integrity analysis. In BPI mode, CCLK is only used in multi-FPGA daisy-chains.

The best signal integrity is ensured by following these basic PCB guidelines:

- Route the CCLK signal as a 50 Ω controlled-impedance transmission line.
- Route the CCLK signal without any branching. Do not use a "star" topology.
- Keep stubs, if required, shorter than 10 mm (0.4 inches).
- Terminate the end of the CCLK transmission line.

Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins

Unlike previous Spartan FPGA families, nearly all of the Spartan-3E dual-purpose configuration pins are available as full-featured user I/O pins after successful configuration, when the DONE output goes High.

The HSWAP pin, the mode select pins (M[2:0]), and the variant-select pins (VS[2:0]) must have valid and stable logic values at the start of configuration. VS[2:0] are only used in the SPI configuration mode. The levels on the M[2:0] pins and VS[2:0] pins are sampled when the INIT_B pin returns High. See Figure 78 for a timing example.

The HSWAP pin defines whether FPGA user I/O pins have a pull-up resistor connected to their associated V_{CCO} supply pin during configuration or not, as shown Table 47. HSWAP must be valid at the start of configuration and remain constant throughout the configuration process.

Table 47: **HSWAP Behavior**

HSWAP Value	Description
0	Pull-up resistors connect to the associated V_{CCO} supply for all user-I/O or dual-purpose I/O pins during configuration. Pull-up resistors are active until configuration completes.
1	Pull-up resistors disabled during configuration. All user-I/O or dual-purpose I/O pins are in a high-impedance state.

The Configuration section provides detailed schematics for each configuration mode. The schematics indicate the required logic values for HSWAP, M[2:0], and VS[2:0] but do not specify how the application provides the logic Low or High value. The HSWAP, M[2:0], and VS[2:0] pins can be either dedicated or reused by the FPGA application.

Dedicating the HSWAP, M[2:0], and VS[2:0] Pins

If the HSWAP, M[2:0], and VS[2:0] pins are not required by the FPGA design after configuration, simply connect these pins directly to the V_{CCO} or GND supply rail shown in the appropriate configuration schematic.

Reusing HSWAP, M[2:0], and VS[2:0] After Configuration

To reuse the HSWAP, M[2:0], and VS[2:0] pin after configuration, use pull-up or pull-down resistors to define the logic values shown in the appropriate configuration schematic.

Table 48: **Pull-up or Pull-down Values for HSWAP, M[2:0], and VS[2:0]**

HSWAP Value	**I/O Pull-up Resistors during Configuration**	**Required Resistor Value to Define Logic Level on HSWAP, M[2:0], or VS[2:0]**	
		High	**Low**
0	Enabled	Pulled High via an internal pull-up resistor to the associated V_{CCO} supply. No external pull-up resistor is necessary.	Pulled Low using an appropriately sized pull-down resistor to GND. For a 2.5V or 3.3V interface: $R \leq 560\ \Omega$. For a 1.8V interface: $R \leq 1.1\ k\Omega$.
1	Disabled	Pulled High using a 3.3 to 4.7 kΩ resistor to the associated V_{CCO} supply.	Pulled Low using a 3.3 to 4.7 kΩ resistor to the associated V_{CCO} supply.

The logic level on HSWAP dictates how to define the logic levels on M[2:0] and VS[2:0], as shown in Table 48. If the application requires HSWAP to be High, the HSWAP pin is pulled High using an external 3.3 to 4.7 kΩ resistor to VCCO_0. If the application requires HSWAP to be Low during configuration, then HSWAP is either connected to GND or pulled Low using an appropriately sized external pull-down resistor to GND. When HSWAP is Low, its pin has an internal pull-up resistor to VCCO_0. The external pull-down resistor must be strong enough to define a logic Low on HSWAP for the I/O standard used during configuration. For 2.5V or 3.3V I/O, the pull-down resistor is 560 Ω or lower. For 1.8V I/O, the pull-down resistor is 1.1 kΩ or lower.

Once HSWAP is defined, use Table 48 to define the logic values for M[2:0] and VS[2:0].

Use the weakest external pull-up or pull-down resistor value allowed by the application. The resistor must be strong enough to define a logic Low or High during configuration. However, when driving the HSWAP, M[2:0], or VS[2:0] pins after configuration, the output driver must be strong enough to overcome the pull-up or pull-down resistor value and generate the appropriate logic levels. For example, to overcome a 560 Ω pull-down resistor, a 3.3V FPGA I/O pin must use a 6 mA or stronger driver.

Master Serial Mode

In Master Serial mode (M[2:0] = <0:0:0>), the Spartan-3E FPGA configures itself from an attached Xilinx Platform Flash PROM, as illustrated in Figure 52. The FPGA supplies the CCLK output clock from its internal oscillator to the attached Platform Flash PROM. In response, the Platform Flash PROM supplies bit-serial data to the FPGA's DIN input, and the FPGA accepts this data on each rising CCLK edge.

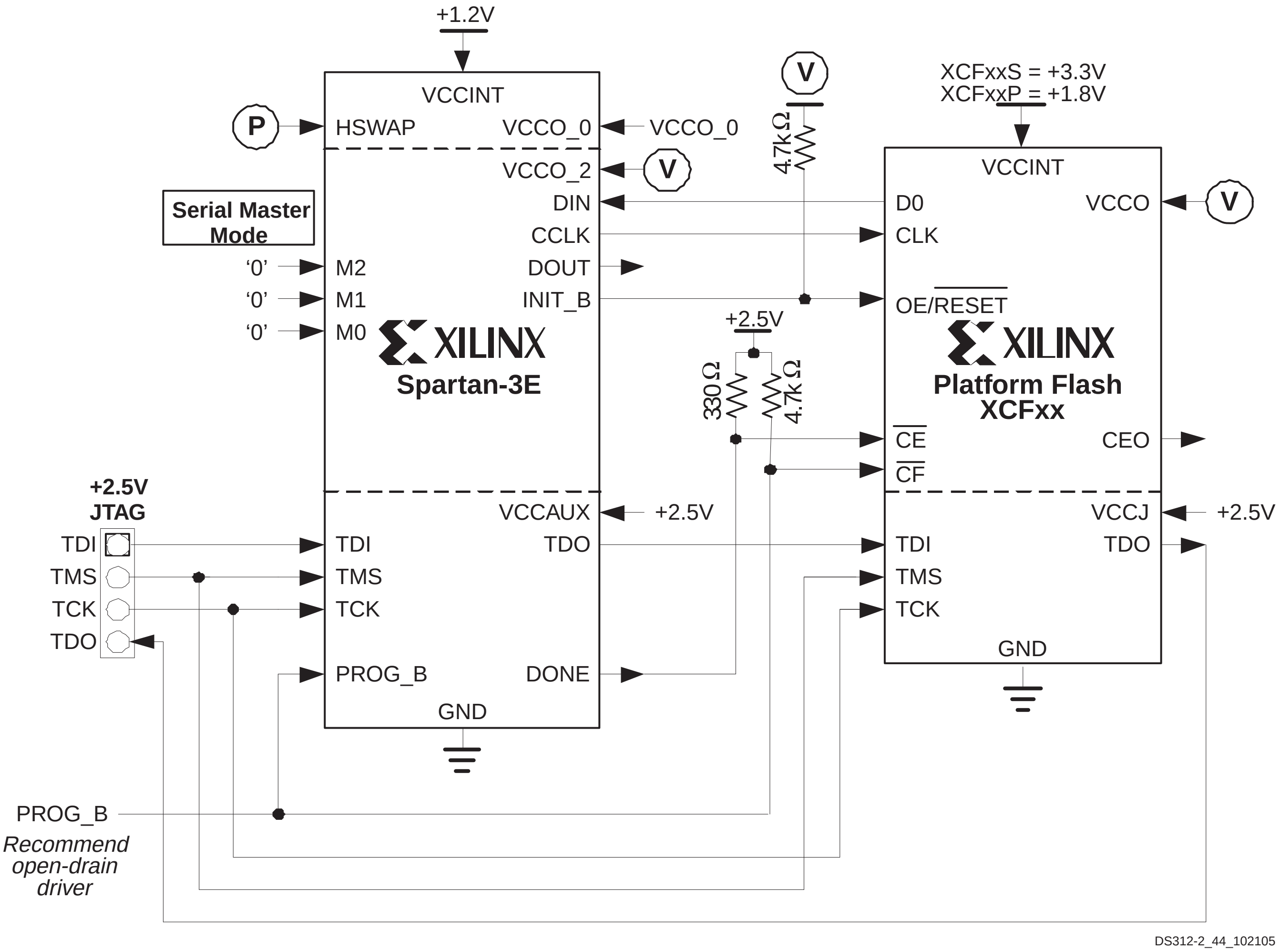


Figure 52: **Master Serial Mode using Platform Flash PROM**

All mode select pins, M[2:0], must be Low when sampled, when the FPGA's INIT_B output goes High. After configuration, when the FPGA's DONE output goes High, the mode select pins are available as full-featured user-I/O pins.

Ⓟ Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins during configuration or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

The FPGA's DOUT pin is used in daisy-chain applications, described later. In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 49: **Serial Master Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP Ⓟ	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See **Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins**.	M2 = 0, M1 = 0, M0 = 0. Sampled when INIT_B goes High.	User I/O
DIN	Input	**Serial Data Input**.	Receives serial data from PROM's D0 output.	User I/O
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See **CCLK Design Considerations**.	Drives PROM's CLK clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. Requires external 4.7 kΩ pull-up resistor to VCCO_2.	Connects to PROM's OE/RESET input. FPGA clears PROM's address counter at start of configuration, enables outputs during configuration. PROM also holds FPGA in Initialization state until PROM reaches Power-On Reset (POR) state. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.

Table 49: **Serial Master Mode Connections *(Continued)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Connects to PROM's chip-enable (CE) input. Enables PROM during configuration. Disables PROM after configuration.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 300 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Requires external 4.7 kΩ pull-up resistor to 2.5V. If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High during configuration to allow configuration to start. Connects to PROM's CF pin, allowing JTAG PROM programming algorithm to reprogram the FPGA.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

The PROM's V_{CCINT} supply must be either 3.3V for the serial XCFxxS Platform Flash PROMs or 1.8V for the serial/parallel XCFxxP PROMs.

Ⓥ The FPGA's VCCO_2 supply input and the Platform Flash PROM's V_{CCO} supply input must be the same voltage, ideally +2.5V. Both devices also support 1.8V and 3.3V interfaces but the FPGA's PROG_B and DONE pins require special attention as they are powered by the FPGA's V_{CCAUX} supply, nominally 2.5V. See application note XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Supported Platform Flash PROMs

Table 50 shows the smallest available Platform Flash PROM to program one Spartan-3E FPGA. A multiple-FPGA daisy-chain application requires a Platform Flash PROM large enough to contain the sum of the various FPGA file sizes.

Table 50: **Number of Bits to Program a Spartan-3E FPGA and Smallest Platform Flash PROM**

Spartan-3E FPGA	Number of Configuration Bits	Smallest Available Platform Flash
XC3S100E	581,344	XCF01S
XC3S250E	1,353,728	XCF02S
XC3S500E	2,270,208	XCF04S
XC3S1200E	3,841,184	XCF04S
XC3S1600E	5,969,696	XCF08P or 2 x XCF04S

The XC3S1600E requires an 8 Mbit PROM. Two solutions are possible: either a single 8 Mbit XCF08P parallel/serial PROM or two 4 Mbit XCF04S serial PROMs cascaded. The two XCF04S PROMs use a 3.3V V_{CCINT} supply while the XCF08P requires a 1.8V V_{CCINT} supply. If the board does not already have a 1.8V supply available, the two cascaded XCF04S PROM solution is recommended.

CCLK Frequency

In Master Serial mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's CLK input pin. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option. Table 51 shows the maximum ***ConfigRate*** settings, approximately equal to MHz, for various Platform Flash devices and I/O voltages. For the serial XCFxxS PROMs, the maximum frequency also depends on the interface voltage.

Table 51: **Maximum ConfigRate Settings for Platform Flash**

Platform Flash Part Number	I/O Voltage ($VCCO\_2$, V_{CCO})	Maximum *ConfigRate* Setting
XCF01S XCF02S XCF04S	3.3V or 2.5V	25
	1.8V	12
XCF08P XCF16P XCF32P	3.3V, 2.5V, or 1.8V	25

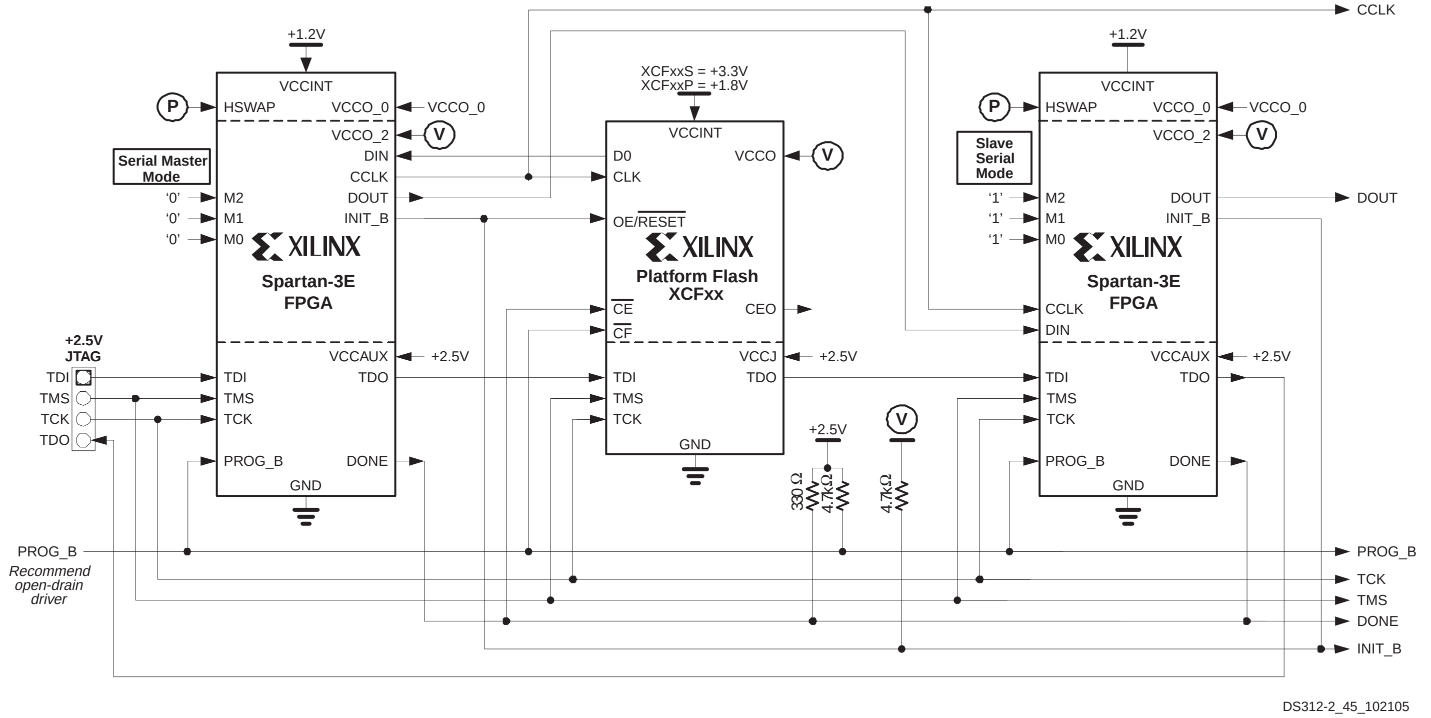


Figure 53: **Daisy-Chaining from Master Serial Mode**

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 53. Use Master Serial mode (M[2:0] = <0:0:0>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the Platform Flash, the master device supplies data using its DOUT output pin to the next device in the daisy-chain, on the falling CCLK edge.

JTAG Interface

Both the Spartan-3E FPGA and the Platform Flash PROM have a four-wire IEEE 1149.1/1532 JTAG port. Both devices share the TCK clock input and the TMS mode select input. The devices may connect in either order on the JTAG chain with the TDO output of one device feeding the TDI input of the following device in the chain. The TDO output of the last device in the JTAG chain drives the JTAG connector.

The JTAG interface on Spartan-3E FPGAs is powered by the 2.5V V_{CCAUX} supply. Consequently, the PROM's V_{CCJ} supply input must also be 2.5V. To create a 3.3V JTAG interface, please refer to application note XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

In-System Programming Support

Both the FPGA and the Platform Flash PROM are in-system programmable via the JTAG chain. Download support is provided by the Xilinx iMPACT programming software and the associated Xilinx Parallel Cable IV, MultiPRO, or Platform Cable USB programming cables.

Storing Additional User Data in Platform Flash

After configuration, the FPGA application can continue to use the Master Serial interface pins to communicate with the Platform Flash PROM. If desired, use a larger Platform Flash PROM to hold additional non-volatile application data, such as MicroBlaze processor code, or other user data such as serial numbers and Ethernet MAC IDs. The FPGA first configures from Platform Flash PROM. Then using FPGA logic after configuration, the FPGA copies MicroBlaze code from Platform Flash into external DDR SDRAM for code execution.

See XAPP694: *Reading User Data from Configuration PROMs* and XAPP482: *MicroBlaze Platform Flash/PROM Boot Loader and User Data Storage* for specific details on how to implement such an interface.

SPI Serial Flash Mode

In SPI Serial Flash mode (M[2:0] = <0:0:1>), the Spartan-3E FPGA configures itself from an attached industry-standard SPI serial Flash PROM, as illustrated in Figure 54 and Figure 55. The FPGA supplies the CCLK output clock from its internal oscillator to the clock input of the attached SPI Flash PROM.

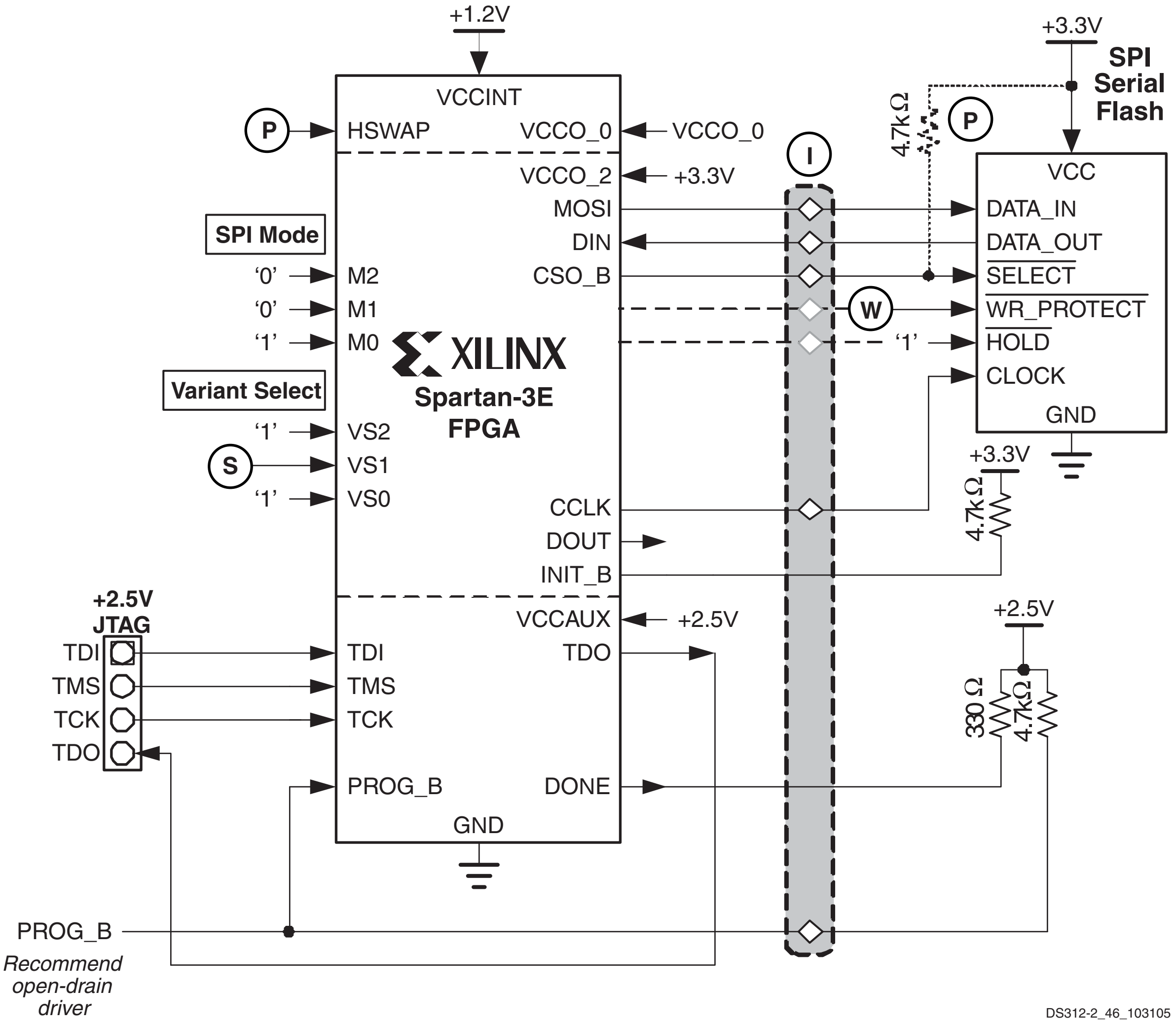


Figure 54: **SPI Flash PROM Interface for PROMs Supporting READ (0x03) and FAST_READ (0x0B) Commands**

Ⓢ Although SPI is a standard four-wire interface, various available SPI Flash PROMs use different command protocols. The FPGA's variant select pins, VS[2:0], define how the FPGA communicates with the SPI Flash, including which SPI Flash command the FPGA issues to start the read operation and the number of dummy bytes inserted before the FPGA expects to receive valid data from the SPI Flash. Table 52 shows the available SPI Flash PROMs expected to operate with Spartan-3E FPGAs. Other compatible devices might work but have not been tested for suitability with Spartan-3E FPGAs. All other VS[2:0] values are reserved for future use. Consult the data sheet for the desired SPI Flash device to determine its suitability. The basic timing requirements and waveforms are provided in **Serial Peripheral Interface (SPI) Configuration Timing** in Module 3.

Figure 54 shows the general connection diagram for those SPI Flash PROMs that support the 0x03 READ command or the 0x0B FAST READ commands.

Figure 55 shows the connection diagram for Atmel DataFlash serial PROMs, which also use an SPI-based protocol. 'B'-series DataFlash devices are limited to FPGA applications operating over the commercial temperature range. Industrial temperature range applications must use 'C'- or 'D'-series DataFlash devices, which have a shorter DataFlash select setup time, because of the faster FPGA CCLK frequency at cold temperatures.

Figure 58, page 84 demonstrates how to configure multiple FPGAs with different configurations, all stored in a single SPI Flash. The diagram uses standard SPI Flash memories but the same general technique applies for Atmel DataFlash.

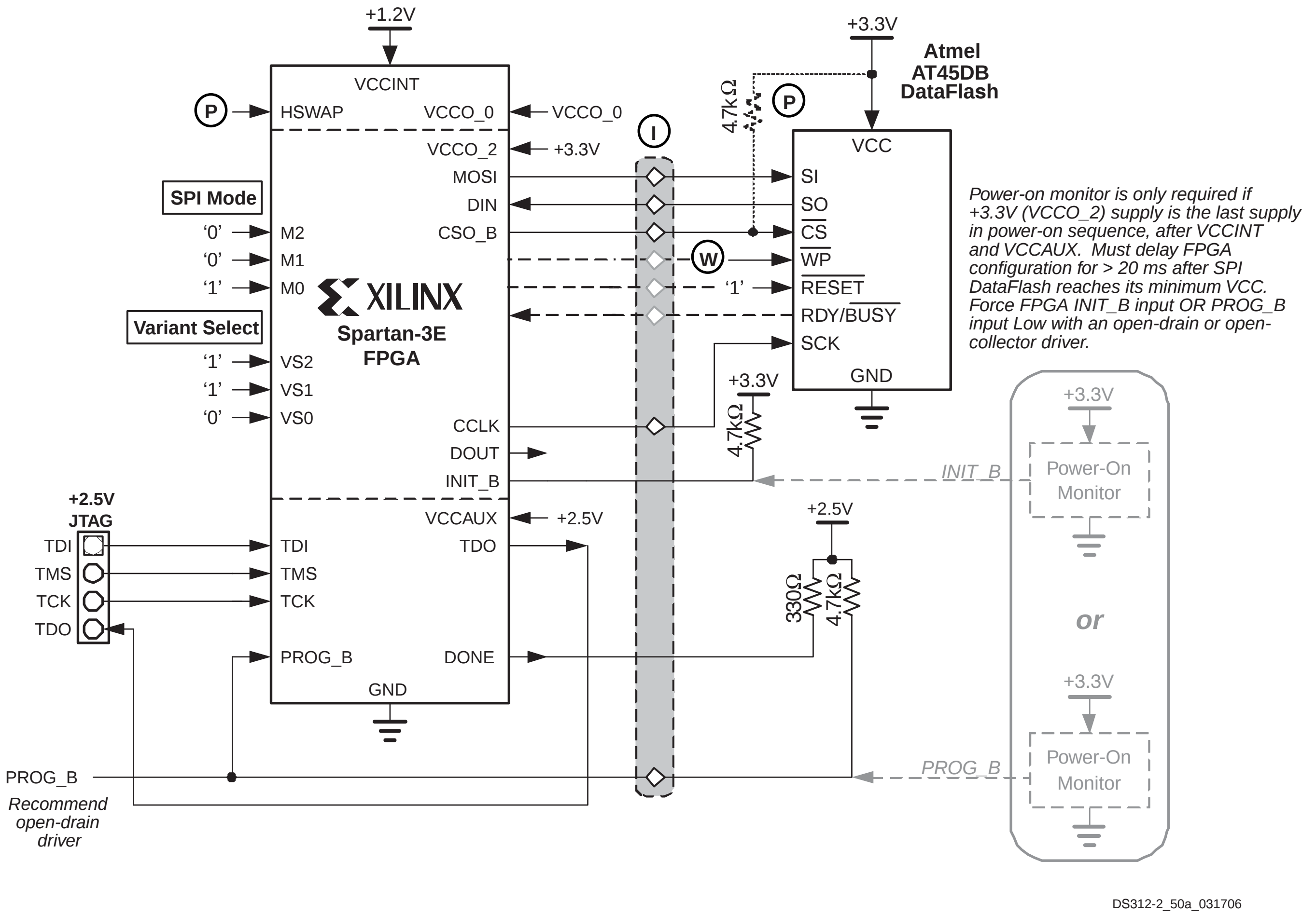


Figure 55: **Atmel SPI-based DataFlash Configuration Interface**

Table 52: **Variant Select Codes for Various SPI Serial Flash PROMs**

VS2	VS1	VS0	SPI Read Command	Dummy Bytes	SPI Serial Flash Vendor	SPI Flash Family	Xilinx Programming Support
1	1	1	FAST READ (0x0B) (see Figure 54)	1	STMicroelectronics (ST)	M25Pxx M25PExx/M45PExx	Yes
					Spansion *(AMD, Fujitsu)*	S25FLxxxA	
					NexFlash / Winbond	NX25Pxx / W25Pxx	
					Macronix	MX25Lxxxx	
					Silicon Storage Technology (SST)	SST25LFxxxA SST25VFxxxA	
					Programmable Microelectronics Corp. (PMC)	Pm25LVxxx	
					Atmel	AT45DB ‘D’-Series Data Flash	Yes
1	0	1	READ (0x03) (see Figure 54)	0	STMicroelectronics (ST)	M25Pxx M25PExx/M45PExx	Yes
					Spansion *(AMD, Fujitsu)*	S25FLxxxA	
					NexFlash / Winbond	NX25Pxx / W25Pxx	
					Macronix	MX25Lxxxx	
					Silicon Storage Technology (SST)	SST25LFxxxA SST25VFxxxA SST25VFxxx	
					Programmable Microelectronics Corp. (PMC)	Pm25LVxxx	
1	1	0	READ ARRAY (0xE8) (see Figure 55)	4	Atmel Corporation	AT45DB DataFlash *(use only ‘C’ or ‘D’ Series for Industrial temperature range)*	Yes
Others			Reserved				

Ⓦ Table 53 shows the connections between the SPI Flash PROM and the FPGA’s SPI configuration interface. Each SPI Flash PROM vendor uses slightly different signal naming. The SPI Flash PROM’s write protect and hold controls are not used by the FPGA during configuration. However, the $\overline{\text{HOLD}}$ pin must be High during the configuration process. The PROM’s write protect input must be High in order to write or program the Flash memory.

Table 53: **Example SPI Flash PROM Connections and Pin Naming**

SPI Flash Pin	FPGA Connection	STMicro	NexFlash	Silicon Storage Technology	Atmel DataFlash
DATA_IN	MOSI	D	DI	SI	SI
DATA_OUT	DIN	Q	DO	SO	SO
$\overline{\text{SELECT}}$	CSO_B	$\overline{\text{S}}$	$\overline{\text{CS}}$	CE#	$\overline{\text{CS}}$
CLOCK	CCLK	C	CLK	SCK	SCK
$\overline{\text{WR\_PROTECT}}$ Ⓦ	Not required for FPGA configuration. Must be High to program SPI Flash. Optional connection to FPGA user I/O after configuration.	$\overline{\text{W}}$	$\overline{\text{WP}}$	WP#	$\overline{\text{WP}}$
$\overline{\text{HOLD}}$ (see Figure 54)	Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Not applicable to Atmel DataFlash.	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$	HOLD#	N/A
$\overline{\text{RESET}}$ (see Figure 55)	Only applicable to Atmel DataFlash. Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Do not connect to FPGA's PROG_B as this will prevent direct programming of the DataFlash.	N/A	N/A	N/A	$\overline{\text{RESET}}$
RDY/$\overline{\text{BUSY}}$ (see Figure 55)	Only applicable to Atmel DataFlash and only available on certain packages. Not required for FPGA configuration. Output from DataFlash PROM. Optional connection to FPGA user I/O after configuration.	N/A	N/A	N/A	RDY/$\overline{\text{BUSY}}$

The mode select pins, M[2:0], and the variant select pins, VS[2:0] are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, these pins are all available as full-featured user-I/O pins.

Ⓟ Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 54: **Serial Peripheral Interface (SPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP Ⓟ	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See **Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins**.	M2 = 0, M1 = 0, M0 = 1. Sampled when INIT_B goes High.	User I/O
VS[2:0] Ⓢ	Input	**Variant Select**. Instructs the FPGA how to communicate with the attached SPI Flash PROM. See **Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins**.	Must be at the logic levels shown in Table 52. Sampled when INIT_B goes High.	User I/O
MOSI	Output	**Serial Data Output**.	FPGA sends SPI Flash memory read commands and starting address to the PROM's serial data input.	User I/O
DIN	Input	**Serial Data Input**.	FPGA receives serial data from PROM's serial data output.	User I/O
CSO_B	Output	**Chip Select Output**. Active Low.	Connects to the SPI Flash PROM's chip-select input. If HSWAP = 1, connect this signal to a 4.7 kΩ pull-up resistor to 3.3V.	Drive CSO_B High after configuration to disable the SPI Flash and reclaim the MOSI, DIN, and CCLK pins. Optionally, re-use this pin and MOSI, DIN, and CCLK to continue communicating with SPI Flash.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See **CCLK Design Considerations**.	Drives PROM's clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O

Table 54: **Serial Peripheral Interface (SPI) Connections *(Continued)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If SPI Flash PROM requires > 2 ms to awake after powering on, hold INIT_B Low until PROM is ready. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 300 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Requires external 4.7 kΩ pull-up resistor to 2.5V. If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to SPI Flash PROM pins.

Voltage Compatibility

Available SPI Flash PROMs use a single 3.3V supply voltage. All of the FPGA's SPI Flash interface signals are within I/O Bank 2. Consequently, the FPGA's VCCO_2 supply voltage must also be 3.3V to match the SPI Flash PROM.

Power-On Precautions if 3.3V Supply is Last in Sequence

Spartan-3E FPGAs have a built-in power-on reset (POR) circuit, as shown in Figure 67. The FPGA waits for its three power supplies — V_{CCINT}, V_{CCAUX}, and V_{CCO} to I/O Bank 2 (VCCO_2) — to reach their respective power-on thresholds before beginning the configuration process.

The SPI Flash PROM is powered by the same voltage supply feeding the FPGA's VCCO_2 voltage input, typically 3.3V. SPI Flash PROMs specify that they cannot be accessed until their V_{CC} supply reaches its minimum data sheet voltage, followed by an additional delay. For some devices, this additional delay is as little as 10 µs as shown in Table 55. For other vendors, this delay is as much as 20 ms.

Table 55: **Example Minimum Power-On to Select Times for Various SPI Flash PROMs**

Vendor	SPI Flash PROM Part Number	Data Sheet Minimum Time from V_{CC} min to Select = Low		
		Symbol	**Value**	**Units**
STMicroelectronics	M25Pxx	T_{VSL}	10	µs
Spansion	S25FLxxxA	t_{PU}	10	ms
NexFlash	NX25xx	T_{VSL}	10	µs
Macronix	MX25Lxxxx	t_{VSL}	10	µs
Silicon Storage Technology	SST25LFxx	$T_{PU\text{-}READ}$	10	µs
Programmable Microelectronics Corporation	Pm25LVxxx	T_{VCS}	50	µs
Atmel Corporation	AT45DBxxxD	t_{VCSL}	30	µs
	AT45DBxxxB		20	ms

In many systems, the 3.3V supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the 3.3V supply feeding the FPGA's VCCO_2 supply is last in the sequence, a potential race occurs between the FPGA and the SPI Flash PROM, as shown in Figure 56.

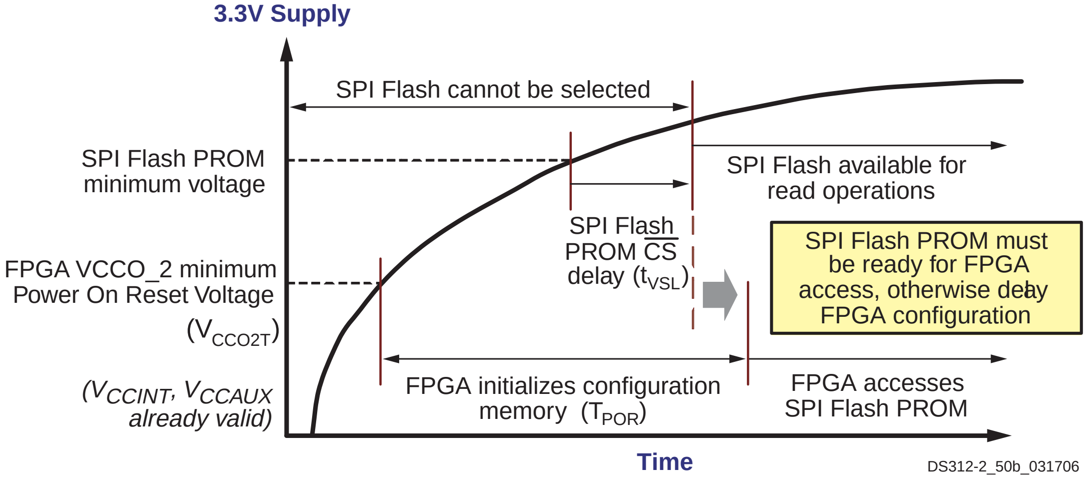


Figure 56: **SPI Flash PROM/FPGA Power-On Timing if 3.3V Supply is Last in Power-On Sequence**

If the FPGA's V_{CCINT} and V_{CCAUX} supplies are already valid, then the FPGA waits for VCCO_2 to reach its minimum threshold voltage before starting configuration. This threshold voltage is labeled as V_{CCO2T} in Table 73 of Module 3 and ranges from approximately 0.4V to 1.0V, substantially lower than the SPI Flash PROM's minimum voltage. Once all three FPGA supplies reach their respective Power On Reset (POR) thresholds, the FPGA starts the configuration process and begins initializing its internal configuration memory. Initialization requires approximately 1 ms (T_{POR}, minimum in Table 108 of Module 3, after which the FPGA deasserts INIT_B, selects the SPI Flash PROM, and starts sending the appropriate read command. The SPI Flash PROM must be ready for read operations at this time.

If the 3.3V supply is last in the sequence and does not ramp fast enough, or if the SPI Flash PROM cannot be ready when required by the FPGA, delay the FPGA configuration process by holding either the FPGA's PROG_B input or INIT_B input Low, as highlighted in Figure 55. Release the FPGA when the SPI Flash PROM is ready. For example, a simple R-C delay circuit attached to the INIT_B pin forces the FPGA to wait for a preselected amount of time. Alternately, a Power Good signal from the 3.3V supply or a system reset signal accomplishes the same purpose. Use an open-drain or open-collector output when driving PROG_B or INIT_B.

SPI Flash PROM Density Requirements

Table 56 shows the smallest usable SPI Flash PROM to program a single Spartan-3E FPGA. Commercially available SPI Flash PROMs range in density from 1 Mbit to 128 Mbits. A multiple-FPGA daisy-chained application requires a SPI Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density SPI Flash PROM to hold additional data beyond just FPGA configuration data. For example, the SPI Flash PROM can also store application code for a MicroBlaze™ RISC processor core integrated in the Spartan-3E FPGA. See **Using the SPI Flash Interface after Configuration**.

Table 56: **Number of Bits to Program a Spartan-3E FPGA and Smallest SPI Flash PROM**

Device	Number of Configuration Bits	Smallest Usable SPI Flash PROM
XC3S100E	581,344	1 Mbit
XC3S250E	1,353,728	2 Mbit
XC3S500E	2,270,208	4 Mbit
XC3S1200E	3,841,184	4 Mbit
XC3S1600E	5,969,696	8 Mbit

CCLK Frequency

In SPI Flash mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's clock input pin. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option. The maximum frequency supported by the FPGA configuration logic depends on the timing for the SPI Flash device. Without examining the timing for a specific SPI Flash PROM, use ***ConfigRate*** = 12 or lower. SPI Flash PROMs that support the FAST READ command support higher data rates. Some such PROMs support up to ***ConfigRate*** = 25 and beyond but require careful data sheet analysis. See **Serial Peripheral Interface (SPI) Configuration Timing** for more detailed timing analysis.

Using the SPI Flash Interface after Configuration

After the FPGA successfully completes configuration, all of the pins connected to the SPI Flash PROM are available as user-I/O pins.

If not using the SPI Flash PROM after configuration, drive CSO_B High to disable the PROM. The MOSI, DIN, and CCLK pins are then available to the FPGA application.

Because all the interface pins are user I/O after configuration, the FPGA application can continue to use the SPI Flash interface pins to communicate with the SPI Flash PROM, as shown in Figure 57. SPI Flash PROMs offer random-accessible, byte-addressable, read/write, non-volatile storage to the FPGA application.

SPI Flash PROMs are available in densities ranging from 1 Mbit up to 128 Mbits. However, a single Spartan-3E FPGA requires less than 6 Mbits. If desired, use a larger SPI Flash PROM to contain additional non-volatile application data, such as MicroBlaze processor code, or other user data such as serial numbers and Ethernet MAC IDs. In the example shown in Figure 57, the FPGA configures from SPI Flash PROM. Then using FPGA logic after configuration, the FPGA copies MicroBlaze code from SPI Flash into external DDR SDRAM for code execution. Similarly, the FPGA application can store non-volatile application data within the SPI Flash PROM.

The FPGA configuration data is stored starting at location 0. Store any additional data beginning in the next available SPI Flash PROM sector or page. Do not mix configuration data and user data in the same sector or page.

Similarly, the SPI bus can be expanded to additional SPI peripherals. Because SPI is a common industry-standard interface, various SPI-based peripherals are available, such as analog-to-digital (A/D) converters, digital-to-analog (D/A) converters, CAN controllers, and temperature sensors.

The MOSI, DIN, and CCLK pins are common to all SPI peripherals. Connect the select input on each additional SPI peripheral to one of the FPGA user I/O pins. If HSWAP = 0 during configuration, the FPGA holds the select line High. If HSWAP = 1, connect the select line to +3.3V via an external 4.7 kΩ pull-up resistor to avoid spurious read or write operations. After configuration, drive the select line Low to select the desired SPI peripheral.

During the configuration process, CCLK is controlled by the FPGA and limited to the frequencies generated by the FPGA. After configuration, the FPGA application can use other clock signals to drive the CCLK pin and can further optimize SPI-based communication.

Refer to the individual SPI peripheral data sheet for specific interface and communication protocol requirements.

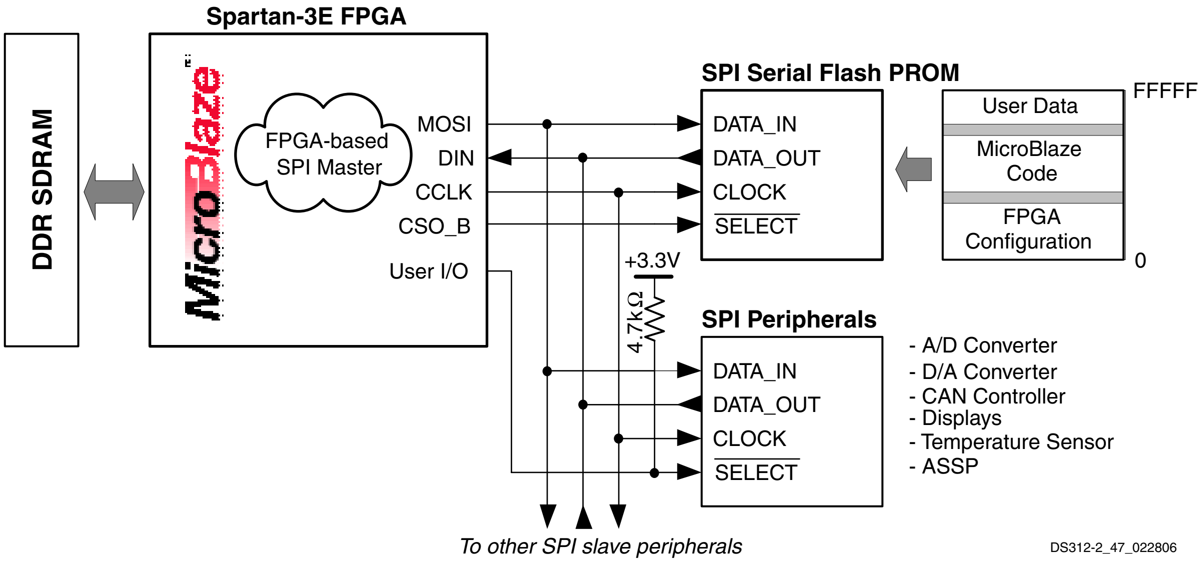


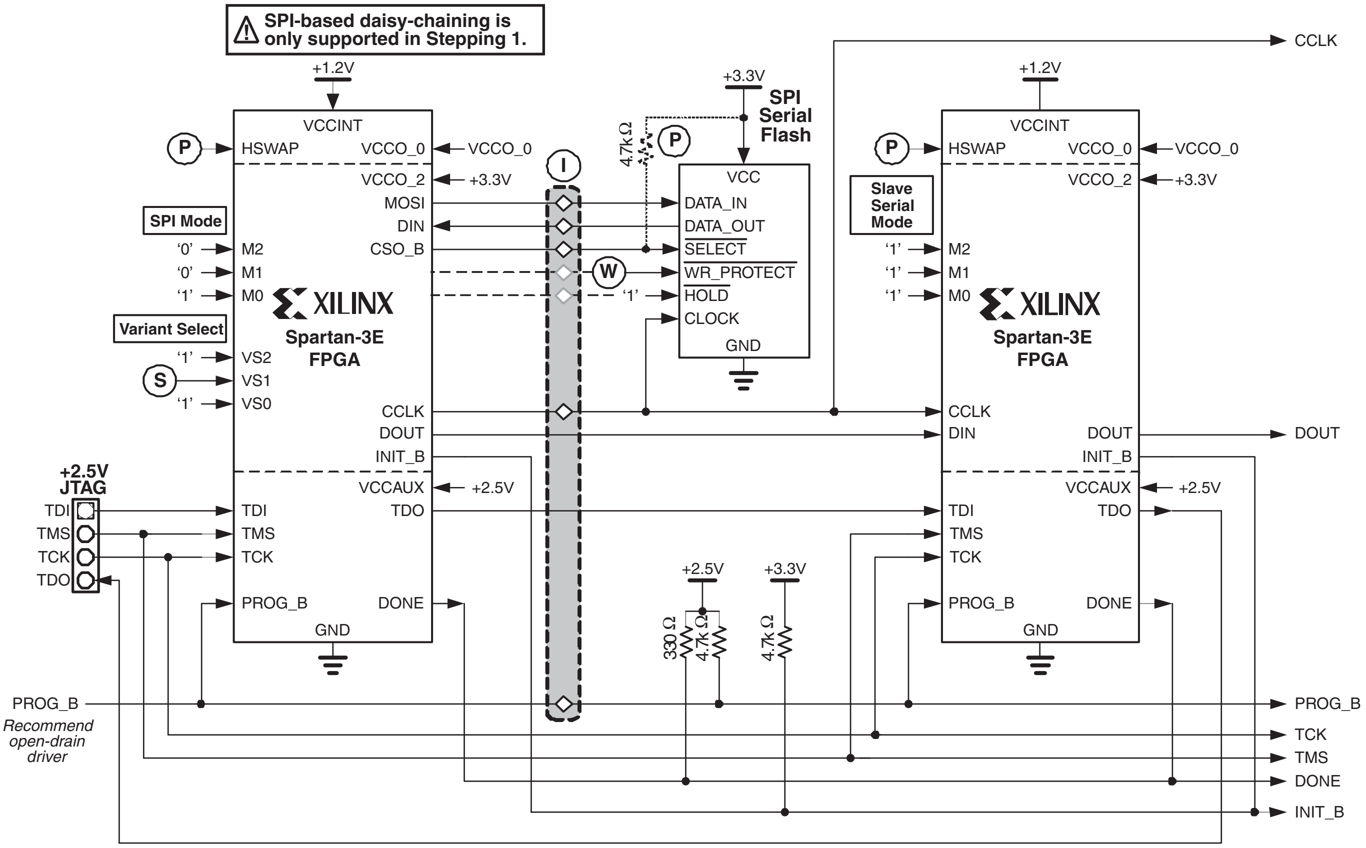
Figure 57: **Using the SPI Flash Interface After Configuration**

Daisy-Chaining

DESIGN NOTE:

SPI mode daisy chains are supported only in Stepping 1 and later silicon versions.

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 58. Daisy-chaining from a single SPI serial Flash PROM is supported in Stepping 1 and later devices. It is not supported in Stepping 0 devices. Use SPI Flash mode (M[2:0] = <0:0:1>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the SPI Flash PROM, the master device uses its DOUT output pin to supply data to the next device in the daisy-chain, on the falling CCLK edge.



DS312-2_48_103105

Figure 58: **Daisy-Chaining from SPI Flash Mode (Stepping 1 and Later)**

Programming Support

For successful daisy-chaining, the ***DONE_cycle*** configuration option must be set to cycle 5 or sooner. The default cycle is 4. See Table 68 and the **Start-Up** section for additional information.

Ⓘ In production applications, the SPI Flash PROM is usually pre-programmed before it is mounted on the printed circuit board. The Xilinx ISE development software produces industry-standard programming files that can be used with third-party gang programmers. Consult your specific SPI Flash vendor for recommended production programming solutions.

In-system programming support is available from some third-party PROM programmers using a socket adapter with attached wires. To gain access to the SPI Flash signals, drive the FPGA's PROG_B input Low with an open-drain driver. This action places all FPGA I/O pins, including those attached to the SPI Flash, in high-impedance (Hi-Z). If the HSWAP input is Low, the I/Os have pull-up resistors to the V_{CCO} input on their respective I/O bank. The external programming hardware then has direct access to the SPI Flash pins. The programming access points are highlighted in the gray box in Figure 54, Figure 55, and Figure 58.

For prototyping purposes, XAPP445 describes how to use the XSPI software and a Xilinx Parallel IV or MultiPro Desktop Tool or other compatible cable to program an attached SPI Flash.

Byte-Wide Peripheral Interface (BPI) Parallel Flash Mode

In Byte-wide Peripheral Interface (BPI) mode (M[2:0] = <0:1:0> or <0:1:1>), a Spartan-3E FPGA configures itself from an industry-standard parallel NOR Flash PROM, as illustrated in Figure 59. The FPGA generates up to a 24-bit address lines to access an attached parallel Flash. Only 20 address lines are generated for Spartan-3E FPGAs in the TQ144 package. Similarly, the XC3S100E FPGA in the CP132 package only has 20 address lines while the XC3S250E and XC3S500E FPGAs in the same package have 24 address lines. When using the VQ100 package, the BPI mode is not available when using parallel NOR Flash, but is supported using parallel Platform Flash (XCFxxP).

The BPI configuration interface is primarily designed for standard parallel NOR Flash PROMs and supports both byte-wide (x8) and byte-wide/halfword (x8/x16) PROMs. The interface functions with halfword-only (x16) PROMs, but the upper byte in a portion of the PROM remains unused. For configuration, the BPI interface does not require any specific Flash PROM features, such as boot block or a specific sector size.

The BPI interface also functions with Xilinx parallel Platform Flash PROMs (XCFxxP), although the FPGA's address lines are left unconnected.

The BPI interface also works equally wells with other asynchronous memories that use a similar SRAM-style interface such as SRAM, NVRAM, EEPROM, EPROM, or masked ROM.

NAND Flash memory is commonly used in memory cards for digital cameras. Spartan-3E FPGAs do not configure directly from NAND Flash memories.

The FPGA's internal oscillator controls the interface timing and the FPGA supplies the clock on the CCLK output pin. However, the CCLK signal is not used in single FPGA applications. Similarly, the FPGA drives three pins Low during configuration (LDC[2:0]) and one pin High during configuration (HDC) to the PROM's control inputs.

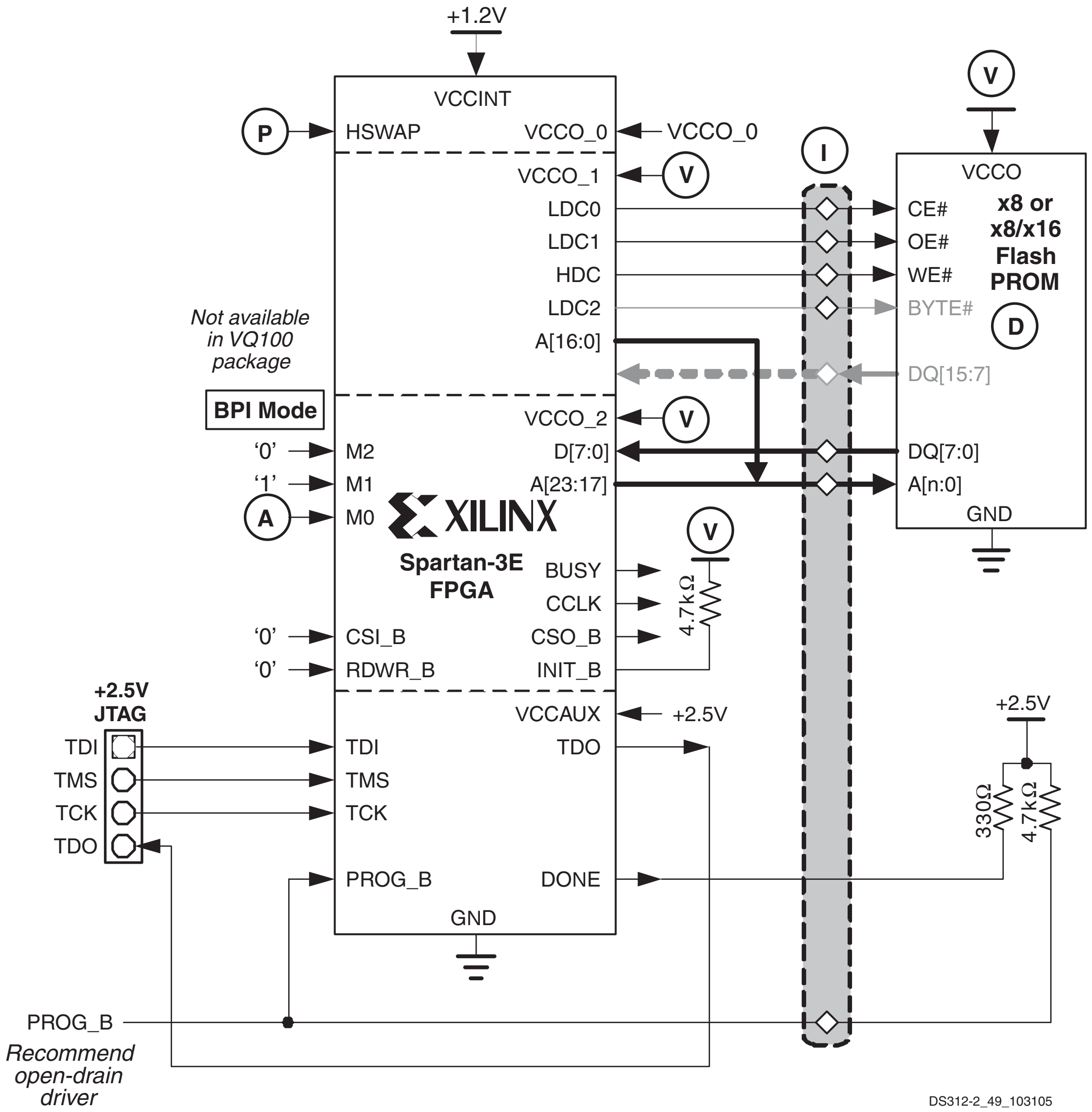


Figure 59: **Byte-wide Peripheral Interface (BPI) Mode Configured from Parallel NOR Flash PROMs**

Ⓐ During configuration, the value of the M0 mode pin determines how the FPGA generates addresses, as shown Table 57. When M0 = 0, the FPGA generates addresses starting at 0 and increments the address on every falling CCLK edge. Conversely, when M0 = 1, the FPGA generates addresses starting at 0xFF_FFFF (all ones) and decrements the address on every falling CCLK edge.

Table 57: **BPI Addressing Control**

M2	M1	M0	Start Address	Addressing
0	1	0	0	Incrementing
		1	0xFF_FFFF	Decrementing

This addressing flexibility allows the FPGA to share the parallel Flash PROM with an external or embedded processor. Depending on the specific processor architecture, the processor boots either from the top or bottom of memory. The FPGA is flexible and boots from the opposite end of memory from the processor. Only the processor or the FPGA can boot at any given time. The FPGA can configure first, holding the processor in reset or the processor can boot first, asserting the FPGA's PROG_B pin.

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

Ⓟ Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

The RDWR_B and CSI_B must be Low throughout the configuration process. After configuration, these pins also become user I/O.

In a single-FPGA application, the FPGA's CSO_B and CCLK pins are not used but are actively driving during the configuration process. The BUSY pin is not used but also actively drives during configuration and is available as a user I/O after configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Furthermore, the bidirectional SelectMAP configuration peripheral interface (see **Slave Parallel Mode**) is available after configuration. To continue using SelectMAP mode, set the ***Persist*** bitstream generator option to ***Yes***. An external host can then read and verify configuration data.

Table 58: **Byte-Wide Peripheral Interface (BPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP Ⓟ	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0] Ⓐ	Input	**Mode Select**. Selects the FPGA configuration mode. See **Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins**.	M2 = 0, M1 = 1. Set M0 = 0 to start at address 0, increment addresses. Set M0 = 1 to start at address 0xFFFFFF and decrement addresses. Sampled when INIT_B goes High.	User I/O
CSI_B	Input	**Chip Select Input**. Active Low.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
RDWR_B	Input	**Read/Write Control**. Active Low write enable. Read functionality typically only used after configuration, if bitstream option ***Persist=Yes***.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
LDC0	Output	PROM Chip Enable	Connect to PROM chip-select input (CE#). FPGA drives this signal Low throughout configuration.	User I/O. If the FPGA does not access the PROM after configuration, drive this pin High to deselect the PROM. A[23:0], D[7:0], LDC[2:1], and HDC then become available as user I/O.
LDC1	Output	PROM Output Enable	Connect to the PROM output-enable input (OE#). The FPGA drives this signal Low throughout configuration.	User I/O

Table 58: **Byte-Wide Peripheral Interface (BPI) Connections *(Continued)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HDC	Output	PROM Write Enable	Connect to PROM write-enable input (WE#). FPGA drives this signal High throughout configuration.	User I/O
LDC2 Ⓓ	Output	PROM Byte Mode	This signal is not used for x8 PROMs. For PROMs with a x8/x16 data width control, connect to PROM byte-mode input (BYTE#). See **Precautions Using x8/x16 Flash PROMs**. FPGA drives this signal Low throughout configuration.	User I/O. Drive this pin High after configuration to use a x8/x16 PROM in x16 mode.
A[23:0]	Output	Address	Connect to PROM address inputs. High-order address lines may not be available in all packages and not all may be required. Number of address lines required depends on the size of the attached Flash PROM. FPGA address generation controlled by M0 mode pin. Addresses presented on falling CCLK edge. Only 20 address lines are available in TQ144 package.	User I/O
D[7:0]	Input	Data Input	FPGA receives byte-wide data on these pins in response the address presented on A[23:0]. Data captured by FPGA	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSO_B	Output	**Chip Select Output**. Active Low.	Not used in single FPGA applications. In a daisy-chain configuration, this pin connects to the CSI_B pin of the next FPGA in the chain. If HSWAP = 1 in a multi-FPGA daisy-chain application, connect this signal to a 4.7 kΩ pull-up resistor to VCCO_2. Actively drives Low when selecting a downstream device in the chain.	User I/O
BUSY	Output	**Busy Indicator**. Typically only used after configuration, if bitstream option ***Persist=Yes***.	Not used during configuration but actively drives.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See **CCLK Design Considerations**.	Not used in single FPGA applications but actively drives. In a daisy-chain configuration, drives the CCLK inputs of all other FPGAs in the daisy-chain.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.

Table 58: **Byte-Wide Peripheral Interface (BPI) Connections *(Continued)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when the mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA is successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 300 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Requires external 4.7 kΩ pull-up resistor to 2.5V. If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to Flash PROM pins.

Voltage Compatibility

Ⓥ The FPGA's parallel Flash interface signals are within I/O Banks 1 and 2. The majority of parallel Flash PROMs use a single 3.3V supply voltage. Consequently, in most cases, the FPGA's VCCO_1 and VCCO_2 supply voltages must also be 3.3V to match the parallel Flash PROM. There are some 1.8V parallel Flash PROMs available and the FPGA interfaces with these devices if the VCCO_1 and VCCO_2 supplies are also 1.8V.

Power-On Precautions if PROM Supply is Last in Sequence

Like SPI Flash PROMs, parallel Flash PROMs typically require some amount of internal initialization time when the supply voltage reaches its minimum value.

The PROM supply voltage also connects to the FPGA's VCCO_2 supply input. In many systems, the PROM supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the PROM supply is last in the sequence, a potential race occurs between the FPGA and the parallel Flash PROM. See **Power-On Precautions if 3.3V Supply is Last in Sequence** for a similar description of the issue for SPI Flash PROMs.

Supported Parallel NOR Flash PROM Densities

Table 59 indicates the smallest usable parallel Flash PROM to program a single Spartan-3E FPGA. Parallel Flash density is specified in bits but addressed as bytes. The FPGA presents up to 24 address lines during configuration but not all are required for single FPGA applications. Table 59 shows the minimum required number of address lines between the FPGA and parallel Flash PROM. The actual number of address line required depends on the density of the attached parallel Flash PROM.

A multiple-FPGA daisy-chained application requires a parallel Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density parallel Flash PROM to hold additional data beyond just FPGA configuration data. For example, the parallel Flash PROM can also contain the application code for a MicroBlaze RISC processor core implemented within the Spartan-3E FPGA. After configuration, the MicroBlaze processor can execute directly from external Flash or can copy the code to other, faster system memory before executing the code.

Table 59: **Number of Bits to Program a Spartan-3E FPGA and Smallest Parallel Flash PROM**

Spartan-3E FPGA	Uncompressed File Sizes (bits)	Smallest Usable Parallel Flash PROM	Minimum Required Address Lines
XC3S100E	581,344	1 Mbit	A[16:0]
XC3S250E	1,353,728	2 Mbit	A[17:0]
XC3S500E	2,270,208	4 Mbit	A[18:0]
XC3S1200E	3,841,184	4 Mbit	A[18:0]
XC3S1600E	5,969,696	8 Mbit	A[19:0]

Compatible Flash Families

The Spartan-3E BPI configuration interface operates with a wide variety of x8 or x8/x16 parallel NOR Flash devices. Table 60 provides a few Flash memory families that operate with the Spartan-3E BPI interface. Consult the data sheet for the desired parallel NOR Flash to determine its suitability The basic timing requirements and waveforms are provided in **Byte Peripheral Interface (BPI) Configuration Timing** (Module 3).

Table 60: **Compatible Parallel NOR Flash Families**

Flash Vendor	Flash Memory Family
ST Microelectronics	M29W
Atmel	AT29 / AT49
Spansion (*AMD, Fujitsu*)	Am29 / S29
Intel	J3 StrataFlash (28F)
Macronix	MX29

CCLK Frequency

In BPI mode, the FPGA's internal oscillator generates the configuration clock frequency that controls all the interface timing. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option.

Table 61: **Maximum ConfigRate Settings for Parallel Flash PROMs (Commercial Temperature Range)**

Flash Read Access Time	Maximum *ConfigRate* Setting
≤ 250 ns	3
≤ 115 ns	6
≤ 45 ns	12

Table 61 shows the maximum ***ConfigRate*** settings for various PROM read access times over the Commercial temperature operating range. See **Byte Peripheral Interface (BPI) Configuration Timing** (Module 3) for more detailed information. Despite using slower ***ConfigRate*** settings, BPI mode is equally fast as the other configuration modes. In BPI mode, data is accessed at the ***ConfigRate*** frequency and internally serialized with an 8X clock frequency.

Using the BPI Interface after Configuration

After the FPGA successfully completes configuration, all pins connected to the parallel Flash PROM are available as user I/Os.

If not using the parallel Flash PROM after configuration, drive LDC0 High to disable the PROM's chip-select input. The remainder of the BPI pins then become available to the FPGA application, including all 24 address lines, the eight data lines, and the LDC2, LDC1, and HDC control pins.

Because all the interface pins are user I/Os after configuration, the FPGA application can continue to use the interface pins to communicate with the parallel Flash PROM. Parallel Flash PROMs are available in densities ranging from 1 Mbit up to 128 Mbits and beyond. However, a single Spartan-3E FPGA requires less than 6 Mbits for configuration. If desired, use a larger parallel Flash PROM to contain additional non-volatile application data, such as MicroBlaze processor code, or other user data, such as serial numbers and Ethernet MAC IDs. In such an example, the FPGA configures from parallel Flash PROM. Then using FPGA logic after configuration, a MicroBlaze processor embedded within the FPGA can either execute code directly from parallel Flash PROM or copy the code to external DDR SDRAM and execute from DDR SDRAM. Similarly, the FPGA application can store non-volatile application data within the parallel Flash PROM.

The FPGA configuration data is stored starting at either at location 0 or the top of memory (addresses all ones) or at both locations for MultiBoot mode. Store any additional data beginning in other available parallel Flash PROM sectors. Do not mix configuration data and user data in the same sector.

Similarly, the parallel Flash PROM interface can be expanded to additional parallel peripherals.

The address, data, and LDC1 (OE#) and HDC (WE#) control signals are common to all parallel peripherals. Connect the chip-select input on each additional peripheral to one of the FPGA user I/O pins. If HSWAP = 0 during configuration, the FPGA holds the chip-select line High via an internal pull-up resistor. If HSWAP = 1, connect the select line to +3.3V via an external 4.7 kΩ pull-up resistor to avoid spurious read or write operations. After configuration, drive the select line Low to select the desired peripheral. Refer to the individual peripheral data sheet for specific interface and communication protocol requirements.

The FPGA optionally supports a 16-bit peripheral interface by driving the LDC2 (BYTE#) control pin High after configuration. See **Precautions Using x8/x16 Flash PROMs** for additional information.

The FPGA provides up to 24 address lines during configuration, addressing up to 128 Mbits (16 Mbytes). If using a larger parallel PROM, connect the upper address lines to FPGA user I/O. During configuration, the upper address lines will be pulled High if HSWAP = 0. Otherwise, use external pull-up or pull-down resistors on these address lines to define their values during configuration.

Precautions Using x8/x16 Flash PROMs

Ⓓ Most low- to mid-density PROMs are byte-wide (x8) only. Many higher-density Flash PROMs support both byte-wide (x8) and halfword-wide (x16) data paths and include a mode input called BYTE# that switches between x8 or x16. During configuration, Spartan-3E FPGAs only support byte-wide data. However, after configuration, the FPGA supports either x8 or x16 modes. In x16 mode, up to eight additional user I/O pins are required for the upper data bits, D[15:8].

Connecting a Spartan-3E FPGA to a x8/x16 Flash PROM is simple, but does require a precaution. Various Flash PROM vendors use slightly different interfaces to support both x8 and x16 modes. Some vendors (Intel, Micron, some STMicroelectronics devices) use a straightforward interface with pin naming that matches the FPGA connections. However, the PROM's A0 pin is wasted in x16 applications and a separate FPGA user-I/O pin is required for the D15 data line. Fortunately, the FPGA A0 pin is still available as a user I/O after configuration, even though it connects to the Flash PROM.

Other vendors (AMD, Atmel, Silicon Storage Technology, some STMicroelectronics devices) use a pin-efficient interface but change the function of one pin, called IO15/A-1, depending if the PROM is in x8 or x16 mode. In x8 mode, BYTE# = 0, this pin is the least-significant address line. The A0 address line selects the halfword location. The A-1 address line selects the byte location. When in x16 mode, BYTE# = 1, the IO15/A-1 pin becomes the most-significant data bit, D15 because byte addressing is not required in this mode. Check to see if the Flash PROM has a pin named "IO15/A-1" or "DQ15/A-1". If so, be careful to connect x8/x16 Flash PROMs correctly, as shown in Table 62. Also, remember that the D[14:8] data connections require FPGA user I/O pins but that the D15 data is already connected for the FPGA's A0 pin.

Table 62: **FPGA Connections to Flash PROM with IO15/A-1 Pin**

FPGA Pin	Connection to Flash PROM with IO15/A-1 Pin	x8 Flash PROM Interface After FPGA Configuration	x16 Flash PROM Interface After FPGA Configuration
LDC2	BYTE#	Drive LDC2 Low or leave unconnected and tie PROM BYTE# input to GND	Drive LCD2 High
LDC1	OE#	Active-Low Flash PROM output-enable control	Active-Low Flash PROM output-enable control
LDC0	CS#	Active-Low Flash PROM chip-select control	Active-Low Flash PROM chip-select control
HDC	WE#	Flash PROM write-enable control	Flash PROM write-enable control
A[23:1]	A[n:0]	A[n:0]	A[n:0]
A0	IO15/A-1	IO15/A-1 is the least-significant address input	IO15/A-1 is the most-significant data line, IO15
D[7:0]	IO[7:0]	IO[7:0]	IO[7:0]
User I/O	Upper data lines IO[14:8] not required unless used as x16 Flash interface after configuration	Upper data lines IO[14:8] not required	IO[14:8]

Some x8/x16 Flash PROMs have a long setup time requirement on the BYTE# signal. For the FPGA to configure correctly, the PROM must be in x8 mode with BYTE# = 0 at power-on or when the FPGA's PROG_B pin is pulsed Low. If required, extend the BYTE# setup time for a 3.3V PROM using an external 680 Ω pull-down resistor on the FPGA's LDC2 pin or by delaying assertion of the CSI_B select input to the FPGA.

Daisy-Chaining

DESIGN NOTE:

⚠ BPI mode daisy chain software support is available starting in ISE 8.2i.

Answer Record #23061
www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=23061

Also, in a multi-FPGA daisy-chain configuration of more than two devices, all intermediate FPGAs between the first and last devices must be Spartan-3E or Virex-5 FPGAs. The last FPGA in the chain can be from any Xilinx FPGA family.

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 60. Use BPI mode (M[2:0] = <0:1:0> or <0:1:1>) for the FPGA connected to the parallel NOR Flash PROM and Slave Parallel mode (M[2:0] = <1:1:0>) for all downstream FPGAs in the daisy-chain. If there are more than two FPGAs in the chain, then last FPGA in the chain can be from any Xilinx FPGA family. However, all intermediate FPGAs located in the chain between the first and last FPGAs must from either the Spartan-3E or Virtex™-5 FPGA families.

After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the parallel Flash PROM, the master device continues generating addresses to the Flash PROM and asserts its CSO_B output Low, enabling the next FPGA in the daisy-chain. The next FPGA then receives parallel configuration data from the Flash PROM. The master FPGA's CCLK output synchronizes data capture.

If HSWAP = 1, an external 4.7kΩ pull-up resistor must be added on the CSO_B pin. If HSWAP = 0, no external pull-up is necessary.

BPI Mode Interaction with Right and Bottom Edge Global Clock Inputs

Some of the BPI mode configuration pins are shared with global clock inputs along the right and bottom edges of the device (Bank 1 and Bank 2, respectively). These pins are not easily reclaimable for clock inputs after configuration, especially if the FPGA application access the parallel NOR Flash after configuration. Table 63 summarizes the shared pins.

Table 63: **Shared BPI Configuration Mode and Global Buffer Input Pins**

Device Edge	Global Buffer Input Pin	BPI Mode Configuration Pin
Bottom	GCLK0	RDWR_B
	GCLK2	D2
	GCLK3	D1
	GCLK12	D7
	GCLK13	D6
	GCLK14	D4
	GCLK15	D3
Right	RHCLK0	A10
	RHCLK1	A9
	RHCLK2	A8
	RHCLK3	A7
	RHCLK4	A6
	RHCLK5	A5
	RHCLK6	A4
	RHCLK7	A3

Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration

The FPGA can always be reprogrammed via the JTAG port, regardless of the mode pin (M[2:0]) settings. However, Stepping 0 devices have a minor limitation. If a Stepping 0 FPGA is set to configure in BPI mode and the FPGA is attached to a parallel memory containing a valid FPGA configuration file, then subsequent reconfigurations using the JTAG port will fail. Potential workarounds include setting the mode pins for JTAG configuration (M[2:0] = <1:0:1>) or offsetting the initial memory location in Flash by 0x2000.

Stepping 1 and later devices fully support JTAG configuration even when the FPGA mode pins are set for BPI mode.

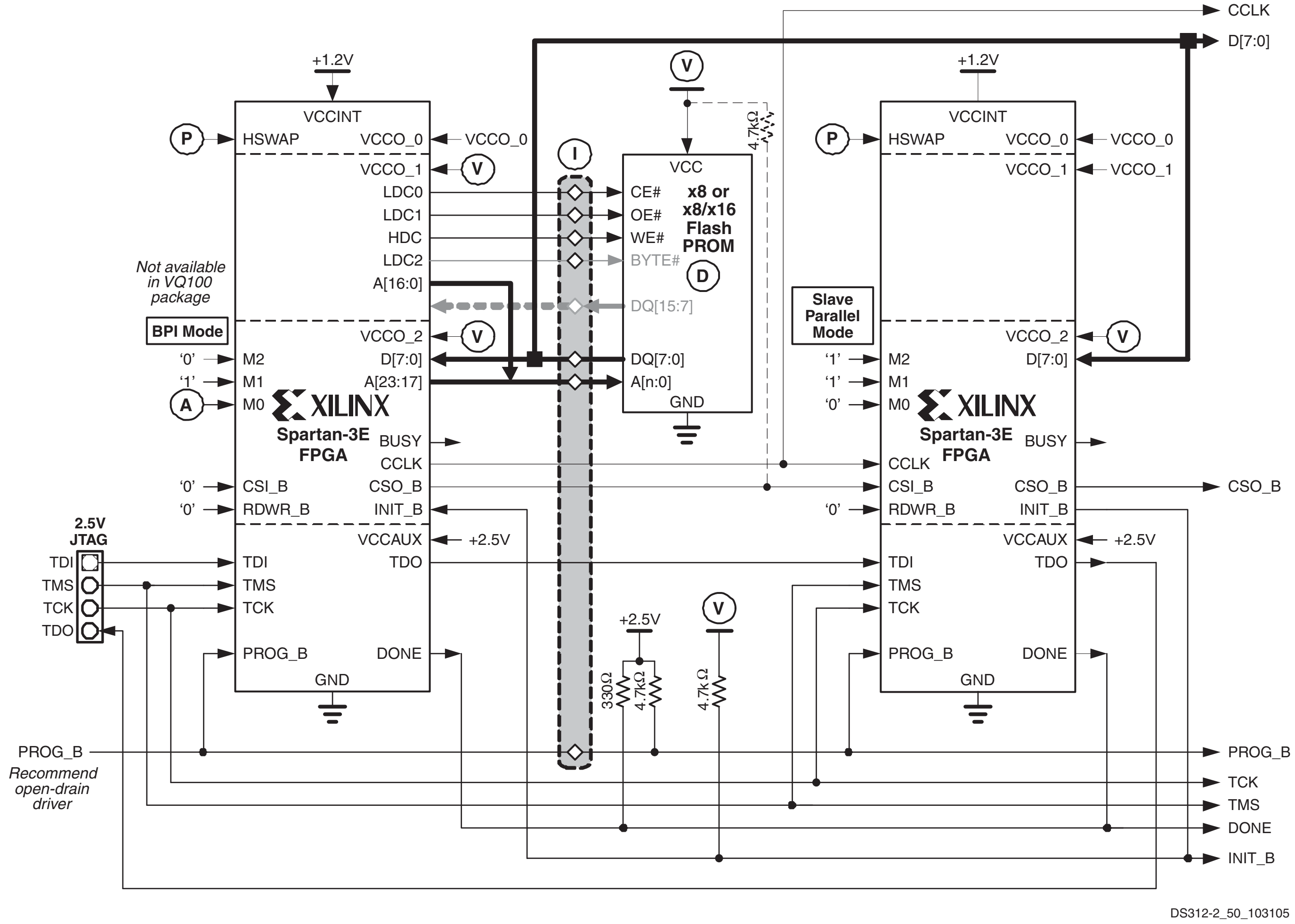


Figure 60: **Daisy-Chaining from BPI Flash Mode**

In-System Programming Support

Ⓘ In a production application, the parallel Flash PROM is usually preprogrammed before it is mounted on the printed circuit board. In-system programming support is available from third-party boundary-scan tool vendors and from some third-party PROM programmers using a socket adapter with attached wires. To gain access to the parallel Flash signals, drive the FPGA's PROG_B input Low with an open-drain driver. This action places all FPGA I/O pins, including those attached to the parallel Flash, in high-impedance (Hi-Z). If the HSWAP input is Low, the I/Os have pull-up resistors to the V_{CCO} input on their respective I/O bank. The external programming hardware then has direct access to the parallel Flash pins. The programming access points are highlighted in the gray boxes in Figure 59 and Figure 60.

The FPGA itself can also be used as a parallel Flash PROM programmer during development and test phases. Initially, an FPGA-based programmer is downloaded into the FPGA via JTAG. Then the FPGA performs the Flash PROM programming algorithms and receives programming data from the host via the FPGA's JTAG interface. See Chapter 11 in Embedded System Tools Reference Manual.

Dynamically Loading Multiple Configuration Images Using MultiBoot Option

After the FPGA configures itself using BPI mode from one end of the parallel Flash PROM, then the FPGA can trigger a MultiBoot event and reconfigure itself from the opposite end of the parallel Flash PROM. MultiBoot is only available when using BPI mode and only for applications with a single Spartan-3E FPGA.

By default, MultiBoot mode is disabled. To trigger a MultiBoot event, assert a Low pulse lasting at least 300 ns on the MultiBoot Trigger (MBT) input to the STARTUP_SPARTAN3E library primitive. When the MBT signal returns High after the 300 ns or longer pulse, the FPGA automatically reconfigures from the opposite end of the parallel Flash memory.

Figure 61 shows an example usage. At power up, the FPGA loads itself from the attached parallel Flash PROM. In this example, the M0 mode pin is Low so the FPGA starts at address 0 and increments through the Flash PROM memory locations. After the FPGA completes configuration, the application initially loaded into the FPGA performs a board-level or system test using FPGA logic. If the test is successful, the FPGA then triggers a MultiBoot event, causing the FPGA to reconfigure from the opposite end of the Flash PROM memory. This second configuration contains the FPGA application for normal operation.

Similarly, the general FPGA application could trigger another MultiBoot event at any time to reload the diagnostics design, and so on.

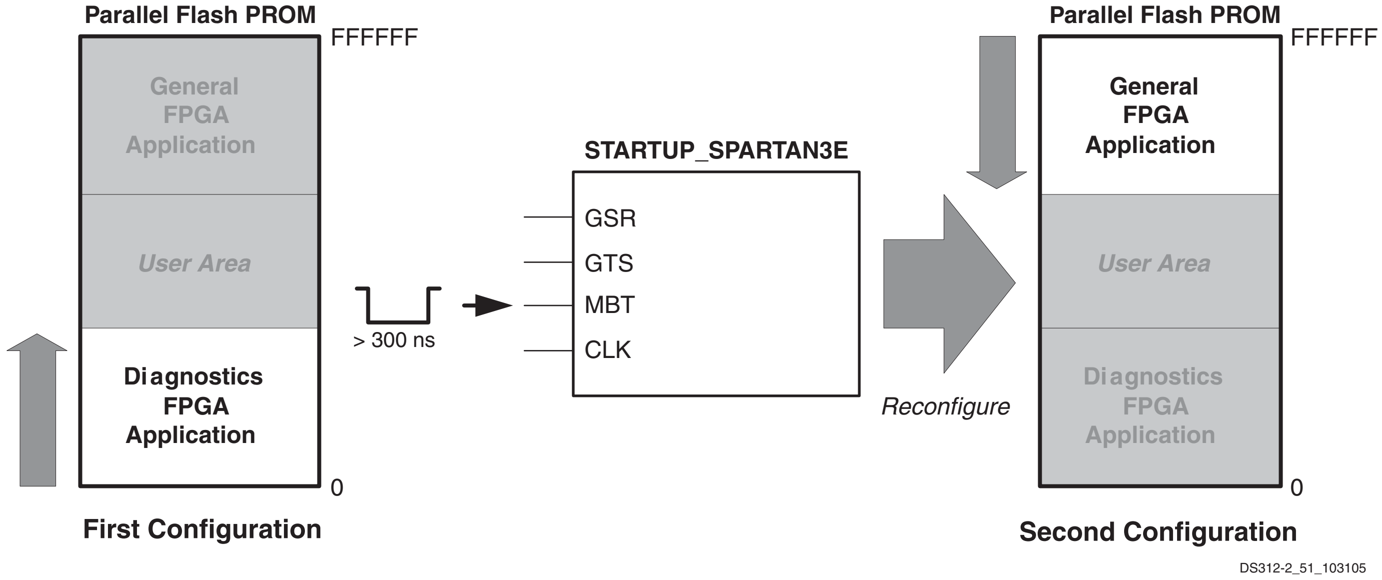


Figure 61: **Use MultiBoot to Load Alternate Configuration Images**

In another potential application, the initial design loaded into the FPGA image contains a “golden” or “fail-safe” configuration image, which then communicates with the outside world and checks for a newer image. If there is a new configuration revision and the new image verifies as good, the “golden” configuration triggers a MultiBoot event to load the new image.

When a MultiBoot event is triggered, the FPGA then again drives its configuration pins as described in Table 58. However, the FPGA does not assert the PROG_B pin. The system design must ensure that no other device drives on these same pins during the reconfiguration process. The FPGA’s DONE, LDC[2:0], or HDC pins can temporarily disable any conflicting drivers during reconfiguration.

Asserting the PROG_B pin Low overrides the MultiBoot feature and forces the FPGA to reconfigure starting from the end of memory defined by the mode pins, shown in Table 57.

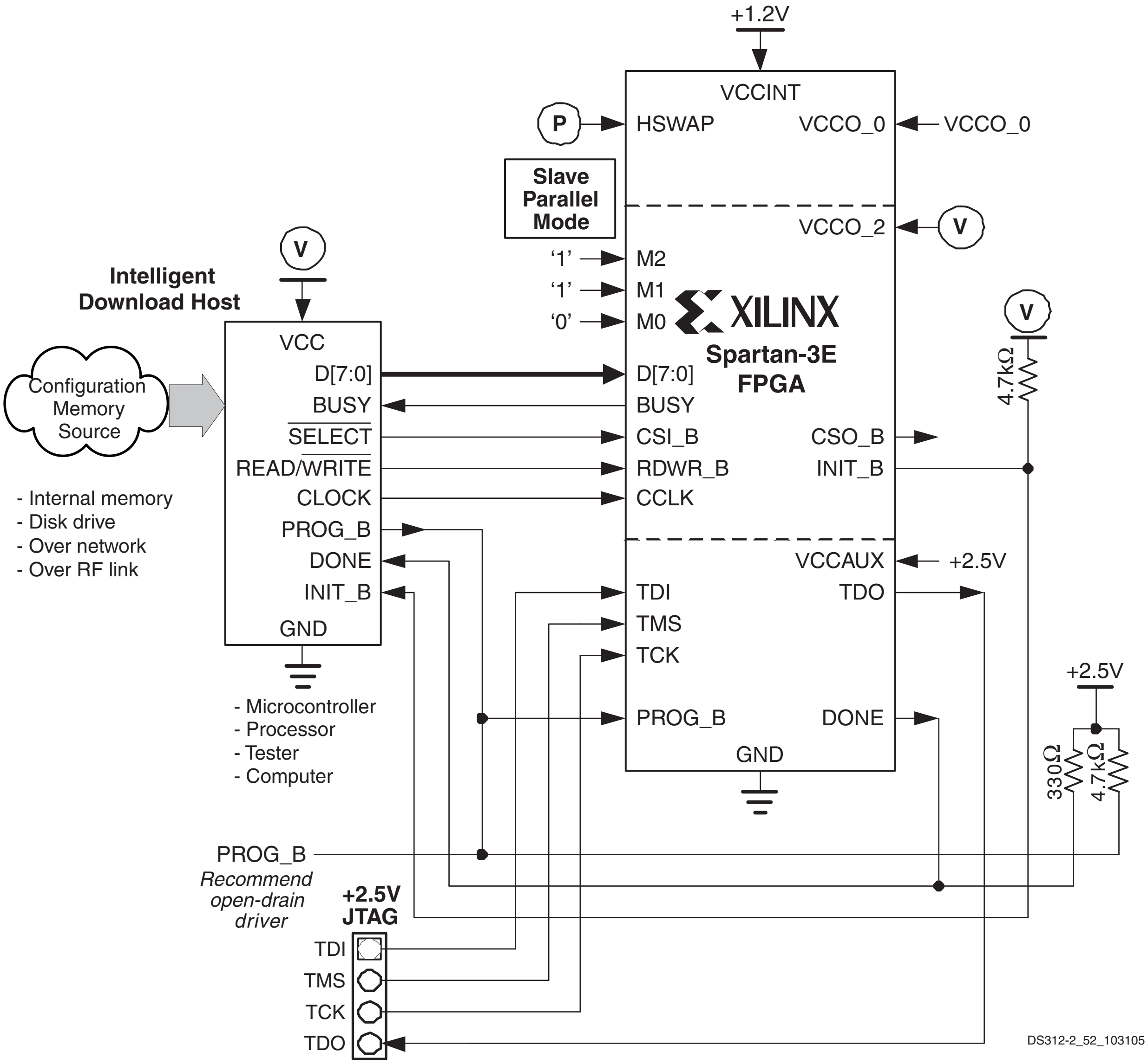


Figure 62: **Slave Parallel Configuration Mode**

Slave Parallel Mode

In Slave Parallel mode (M[2:0] = <1:1:0>), an external host, such as a microprocessor or microcontroller, writes byte-wide configuration data into the FPGA, using a typical peripheral interface as shown in Figure 62.

The external download host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host asserts the active-Low chip-select signal (CSI_B) and the active-Low Write signal (RDWR_B). The host then continues supplying data and clock signals until either the FPGA's DONE pin goes High, indicating a successful configuration, or until the FPGA's INIT_B pin goes Low, indicating a configuration error.

The FPGA captures data on the rising CCLK edge. If the CCLK frequency exceeds 50 MHz, then the host must also monitor the FPGA's BUSY output. If the FPGA asserts BUSY High, the host must hold the data for an additional clock cycle, until BUSY returns Low. If the CCLK frequency is 50 MHz or below, the BUSY pin may be ignored but actively drives during configuration.

The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA's start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see **Start-Up**, page 107).

If the Slave Parallel interface is only used to configure the FPGA, never to read data back, then the RDWR_B signal can also be eliminated from the interface. However, RDWR_B must remain Low during configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Alternatively, the bidirectional SelectMAP configuration interface is available after configuration. To continue using SelectMAP mode, set the ***Persist*** bitstream generator option to ***Yes***. The external host can then read and verify configuration data.

The Slave Parallel mode is also used with BPI mode to create multi-FPGA daisy-chains. The lead FPGA is set for BPI mode configuration; all the downstream daisy-chain FPGAs are set for Slave Parallel configuration, as highlighted in Figure 60.

Table 64: **Slave Parallel Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See **Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins**.	M2 = 1, M1 = 1, M0 = 0 Sampled when INIT_B goes High.	User I/O
D[7:0]	Input	**Data Input**.	Byte-wide data provided by host. FPGA captures data on rising CCLK edge.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
BUSY	Output	**Busy Indicator**.	If CCLK frequency is < 50 MHz, this pin may be ignored. When High, indicates that the FPGA is not ready to receive additional configuration data. Host must hold data an additional clock cycle.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSI_B	Input	**Chip Select Input**. Active Low.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
RDWR_B	Input	**Read/Write Control**. Active Low write enable.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CCLK	Input	**Configuration Clock**. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See **CCLK Design Considerations**.	External clock.	User I/O If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSO_B	Output	**Chip Select Output**. Active Low.	Not used in single FPGA applications. In a daisy-chain configuration, this pin connects to the CSI_B pin of the next FPGA in the chain. Actively drives.	User I/O

Table 64: **Slave Parallel Mode Connections *(Continued)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 300 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Requires external 4.7 kΩ pull-up resistor to 2.5V. If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

Ⓥ Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

The LDC[2:0] and HDC signal are active in I/O Bank 1 but are not used in the interface. Consequently, VCCO_1 can be set the appropriate voltage for the application.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in Figure 63 is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting is chip-select output, CSO_B.

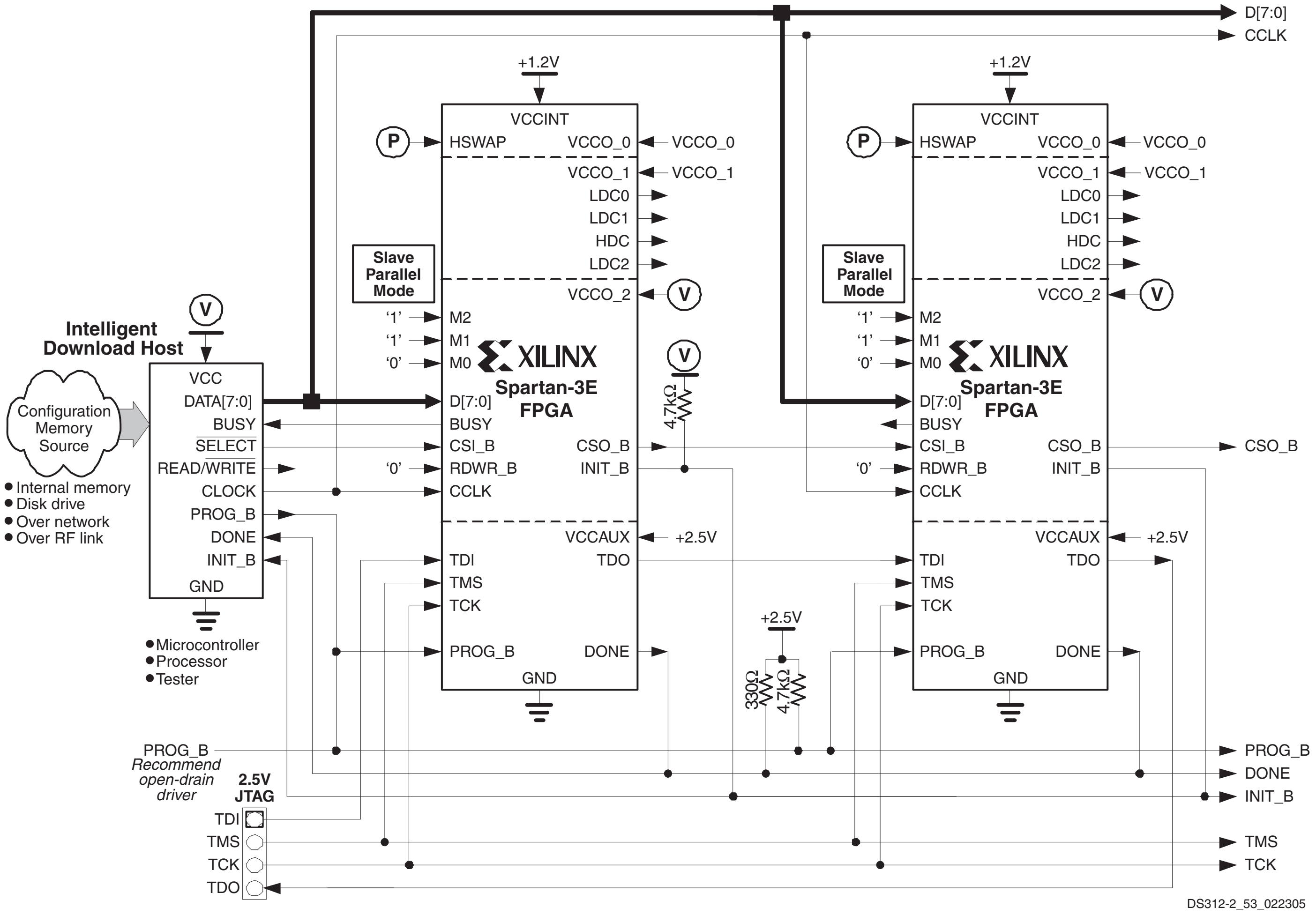


Figure 63: **Daisy-Chaining using Slave Parallel Mode**

Slave Serial Mode

In Slave Serial mode (M[2:0] = <1:1:1>), an external host such as a microprocessor or microcontroller writes serial configuration data into the FPGA, using the synchronous serial interface shown in Figure 64. The serial configuration data is presented on the FPGA's DIN input pin with sufficient setup time before each rising edge of the externally generated CCLK clock input.

The intelligent host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host then continues supplying data and clock signals until either the DONE pin goes High, indicating a successful configuration, or until the INIT_B pin goes Low, indicating a configuration error. The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA's start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see **Start-Up**, page 107).

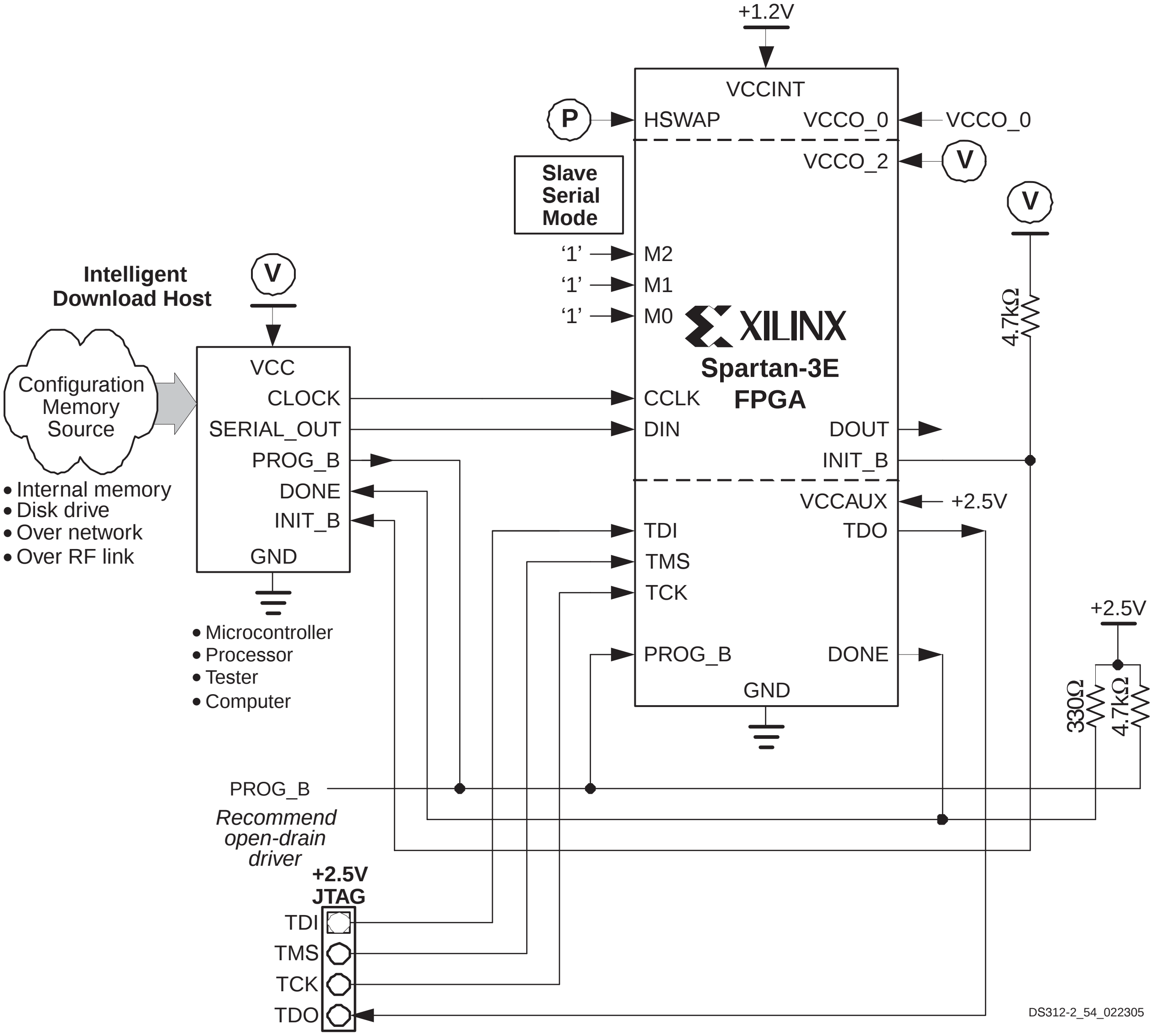


Figure 64: **Slave Serial Configuration**

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

Ⓟ Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

Voltage Compatibility

Ⓥ Most Slave Serial interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 3.3V, 2.5V, or 1.8V to match the requirements of the external host, ideally 2.5V. Using 3.3V or 1.8V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 65. Use Slave Serial mode (M[2:0] = <1:1:1>) for all FPGAs in the daisy-chain. After the lead FPGA is filled with its configuration data, the lead FPGA passes configuration data via its DOUT output pin to the next FPGA on the falling CCLK edge.

Table 65: **Slave Serial Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-up during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See **Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins**.	M2 = 1, M1 = 1, M0 = 1 Sampled when INIT_B goes High.	User I/O
DIN	Input	**Data Input**.	Serial data provided by host. FPGA captures data on rising CCLK edge.	User I/O
CCLK	Input	**Configuration Clock**. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See **CCLK Design Considerations**.	External clock.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 300 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Requires external 4.7 kΩ pull-up resistor to 2.5V. If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

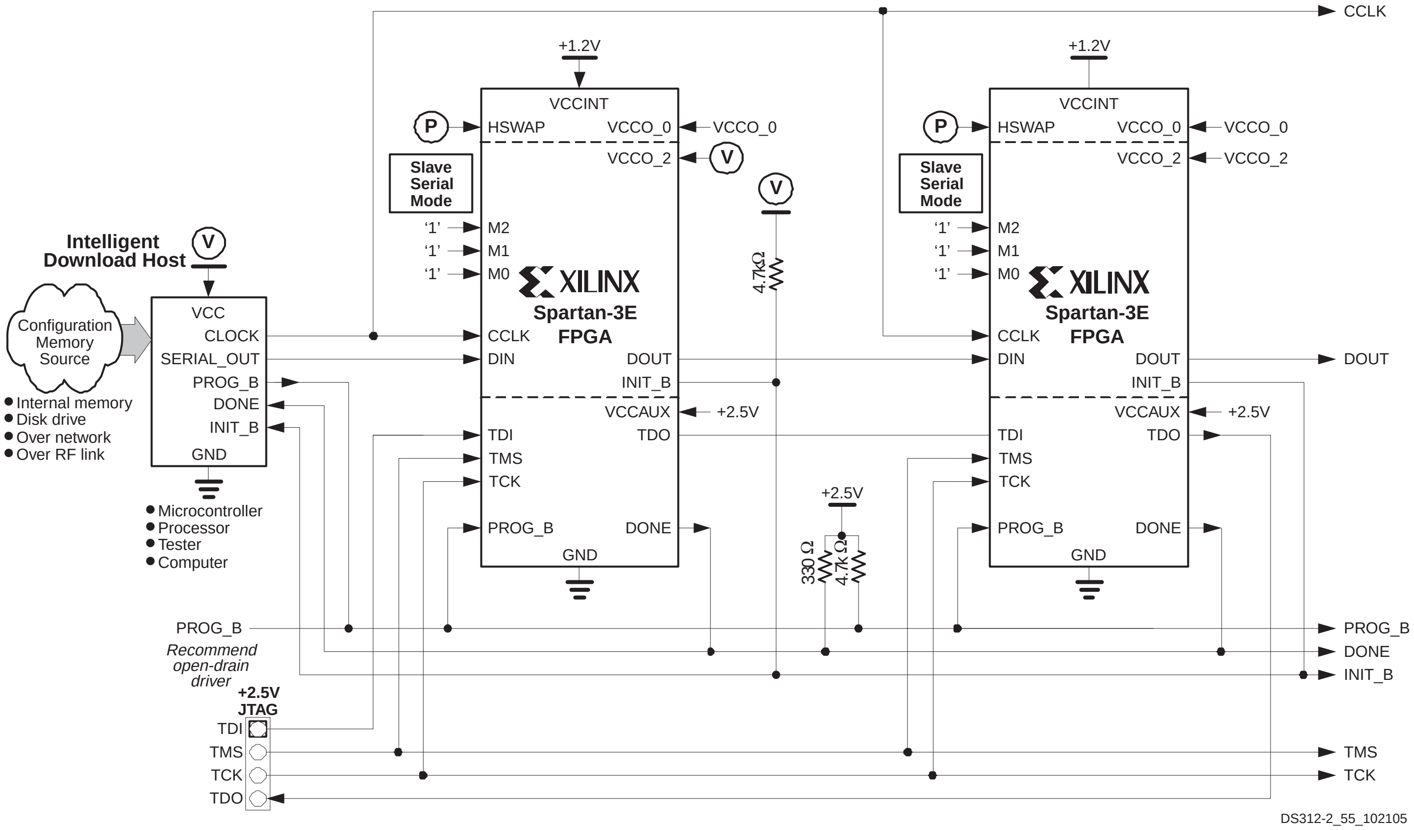


Figure 65: **Daisy-Chaining using Slave Serial Mode**

JTAG Mode

The Spartan-3E FPGA has a dedicated four-wire IEEE 1149.1/1532 JTAG port that is always available any time the FPGA is powered and regardless of the mode pin settings. However, when the FPGA mode pins are set for JTAG mode (M[2:0] = <1:0:1>), the FPGA waits to be configured via the JTAG port after a power-on event or when PROG_B is asserted. Selecting the JTAG mode simply disables the other configuration modes. No other pins are required as part of the configuration interface.

Figure 66 illustrates a JTAG-only configuration interface. The JTAG interface is easily cascaded to any number of FPGAs by connecting the TDO output of one device to the TDI input of the next device in the chain. The TDO output of the last device in the chain loops back to the port connector.

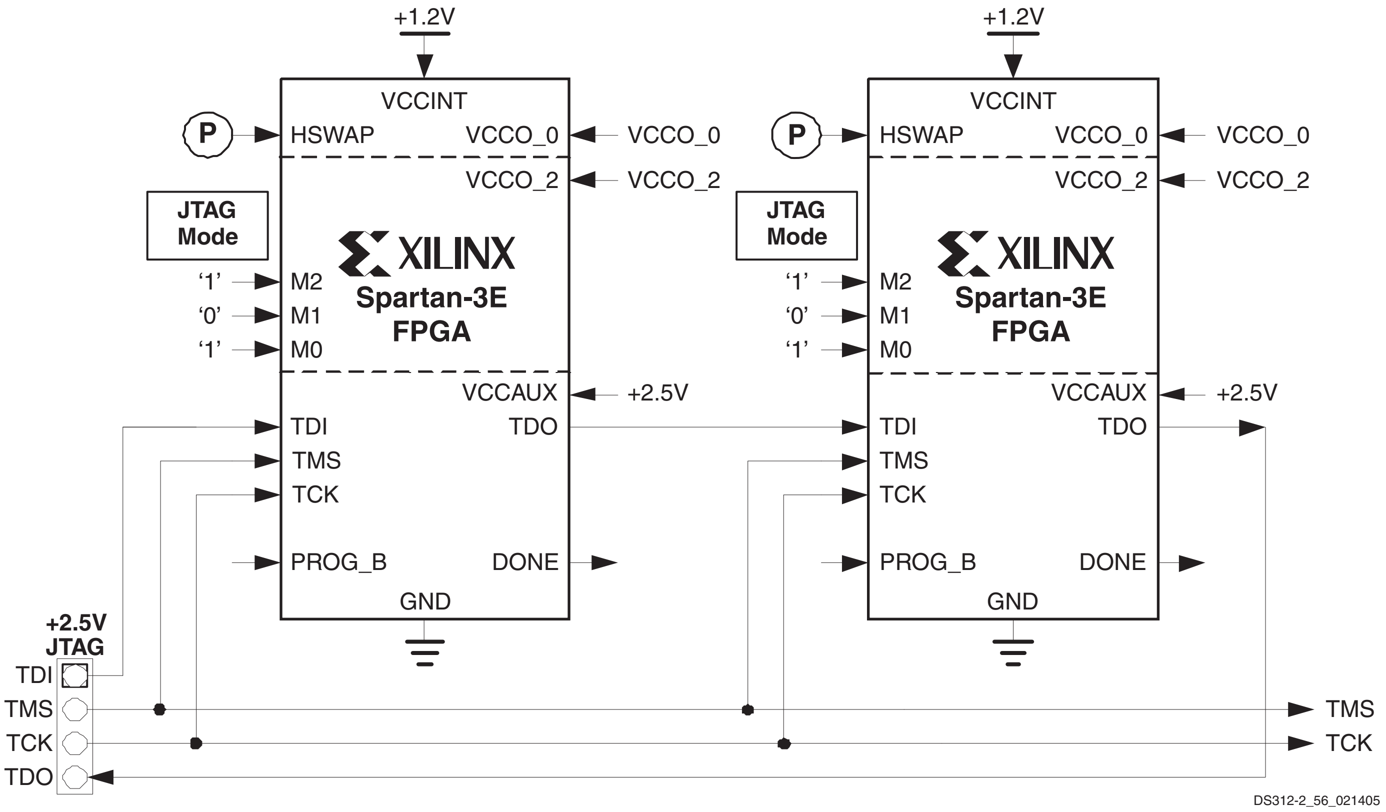


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Figure 66: **JTAG Configuration Mode**

Voltage Compatibility

The 2.5V V_{CCAUX} supply powers the JTAG interface. All of the user I/Os are separately powered by their respective VCCO_# supplies.

When connecting the Spartan-3E JTAG port to a 3.3V interface, the JTAG input pins must be current-limited to 10 mA or less using series resistors. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Table 66: **Spartan-3E JTAG Device Identifiers**

Spartan-3E FPGA	4-Bit Revision Code		28-Bit Vendor/Device Identifier
	Step 0	Step 1	
XC3S100E	0x0	0x1	0x1C 10 093
XC3S250E	0x0	0x1	0x1C 1A 093
XC3S500E	0x0 0x2	0x4	0x1C 22 093
XC3S1200E	0x0 0x1		0x1C 2E 093
XC3S1600E	0x0 0x1	0x2	0x1C 3A 093

JTAG Device ID

Each Spartan-3E FPGA array type has a 32-bit device-specific JTAG device identifier as shown in Table 66. The lower 28 bits represent the device vendor (Xilinx) and device identifier. The upper four bits, ignored by most tools, represent the revision level of the silicon mounted on the printed circuit board. Table 66 associates the revision code with a specific stepping level.

JTAG User ID

The Spartan-3E JTAG interface also provides the option to store a 32-bit User ID, loaded during configuration. The User ID value is specified via the ***UserID*** configuration bitstream option, shown in Table 68, page 108.

Using JTAG Interface to Communicate to a Configured FPGA Design

After the FPGA is configured, using any of the available modes, the JTAG interface offers a possible communications channel to internal FPGA logic. The BSCAN_SPARTAN3 design primitive provides two private JTAG instructions to create an internal boundary scan chain.

Maximum Bitstream Size for Daisy-Chains

The maximum bitstream length supported by Spartan-3E FPGAs in serial daisy-chains is 4,294,967,264 bits

(4 Gbits), roughly equivalent to a daisy-chain with 720 XC3S1600E FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.

Configuration Sequence

The Spartan-3E configuration process is three-stage process that begins after the FPGA powers on (a POR event) or after the PROG_B input is asserted. Power-On Reset (POR) occurs after the V_{CCINT}, V_{CCAUX}, and the V_{CCO} Bank 2 supplies reach their respective input threshold levels. After either a POR or PROG_B event, the three-stage configuration process begins.

1. The FPGA clears (initializes) the internal configuration memory.
2. Configuration data is loaded into the internal memory.
3. The user-application is activated by a start-up process.

Figure 67 is a generalized block diagram of the Spartan-3E configuration logic, showing the interaction of different device inputs and Bitstream Generator (BitGen) options. A flow diagram for the configuration sequence of the Serial and Parallel modes appears in Figure 68. Figure 69 shows the Boundary-Scan or JTAG configuration sequence.

Initialization

Configuration automatically begins after power-on or after asserting the FPGA PROG_B pin, unless delayed using the FPGA's INIT_B pin. The FPGA holds the open-drain INIT_B signal Low while it clears its internal configuration memory. Externally holding the INIT_B pin Low forces the configuration sequencer to wait until INIT_B again goes High.

The FPGA signals when the memory-clearing phase is complete by releasing the open-drain INIT_B pin, allowing the pin to go High via the external pull-up resistor to VCCO_2.

Loading Configuration Data

After initialization, configuration data is written to the FPGA's internal memory. The FPGA holds the Global Set/Reset (GSR) signal active throughout configuration, holding all FPGA flip-flops in a reset state. The FPGA signals when the entire configuration process completes by releasing the DONE pin, allowing it to go High.

The FPGA configuration sequence can also be initiated by asserting PROG_B. Once released, the FPGA begins clearing its internal configuration memory, and progresses through the remainder of the configuration process.

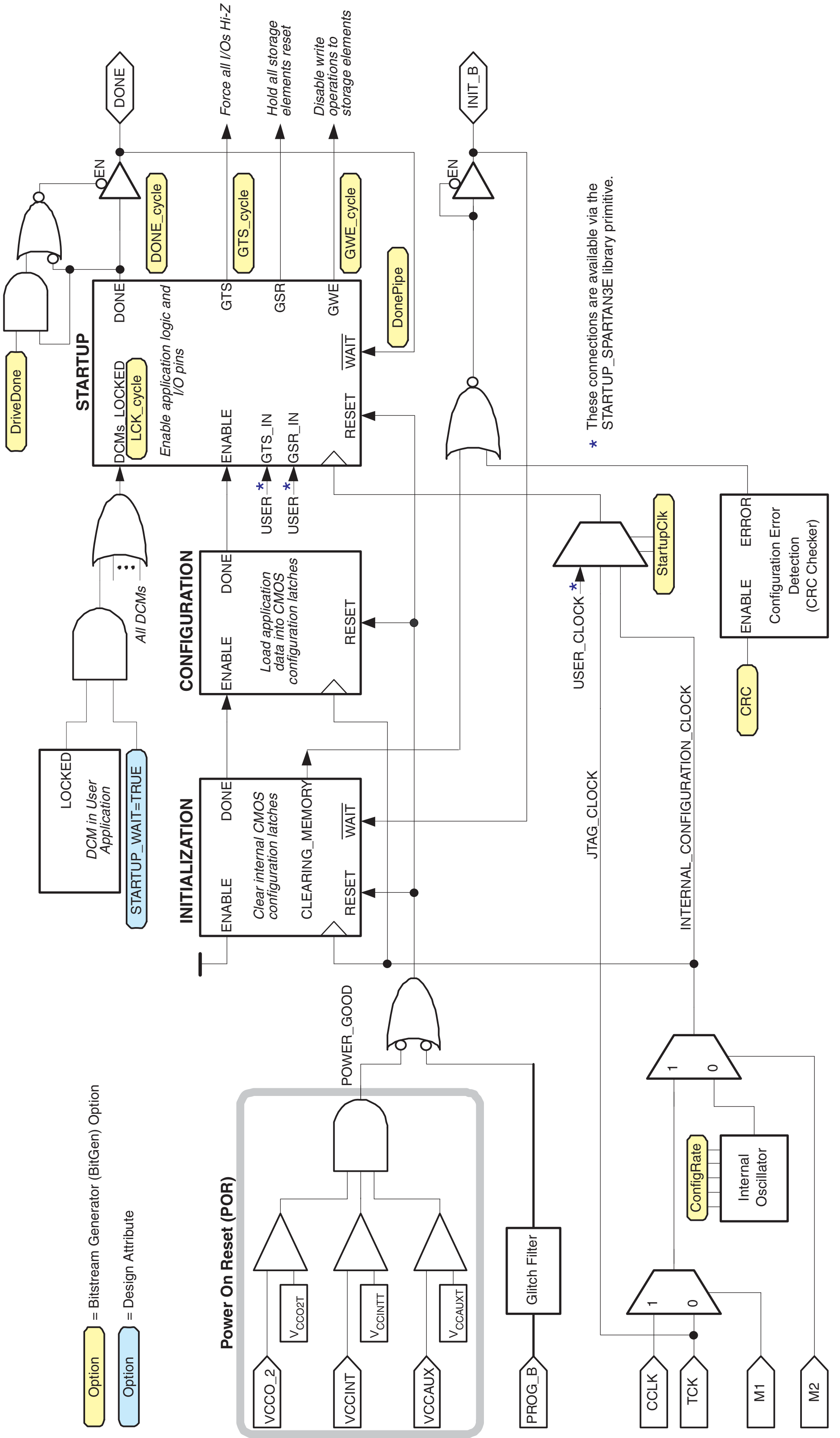

Figure 67: **Generalized Spartan-3E FPGA Configuration Logic Block Diagram**

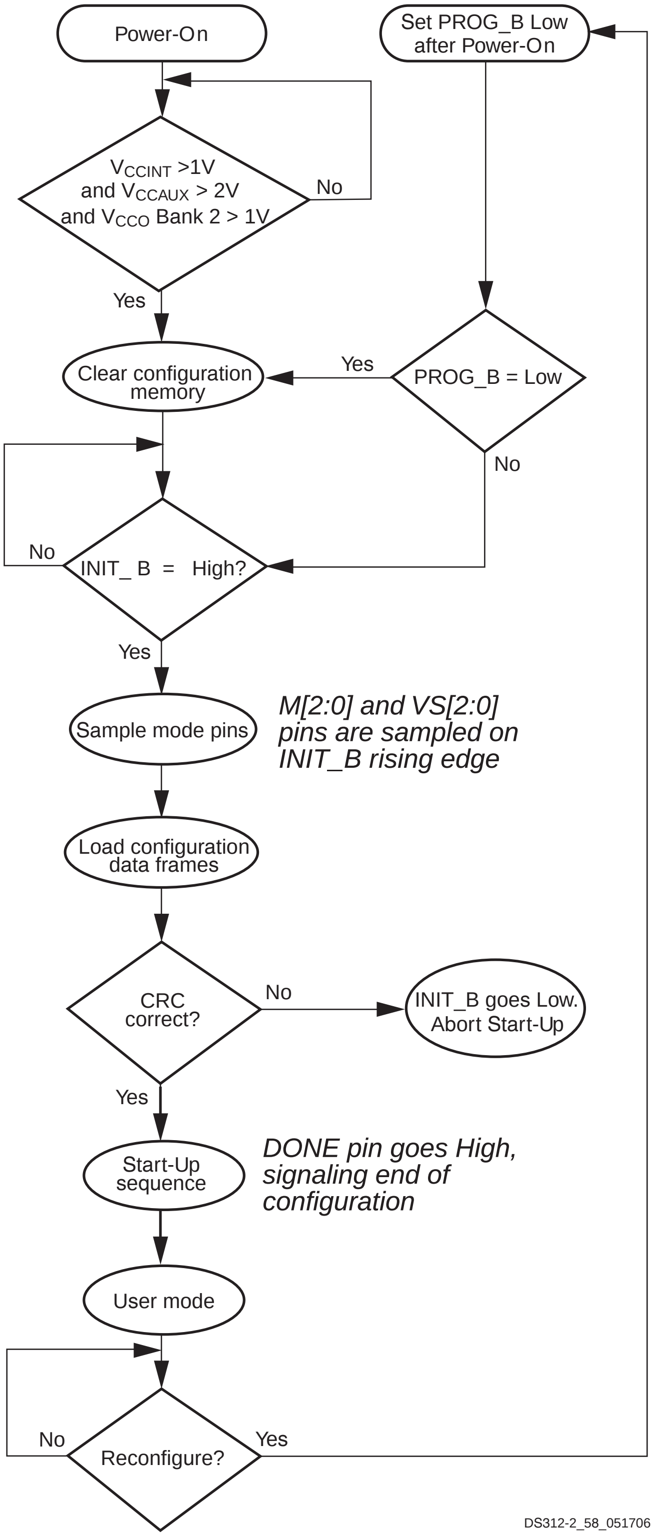

Figure 68: **General Configuration Process**

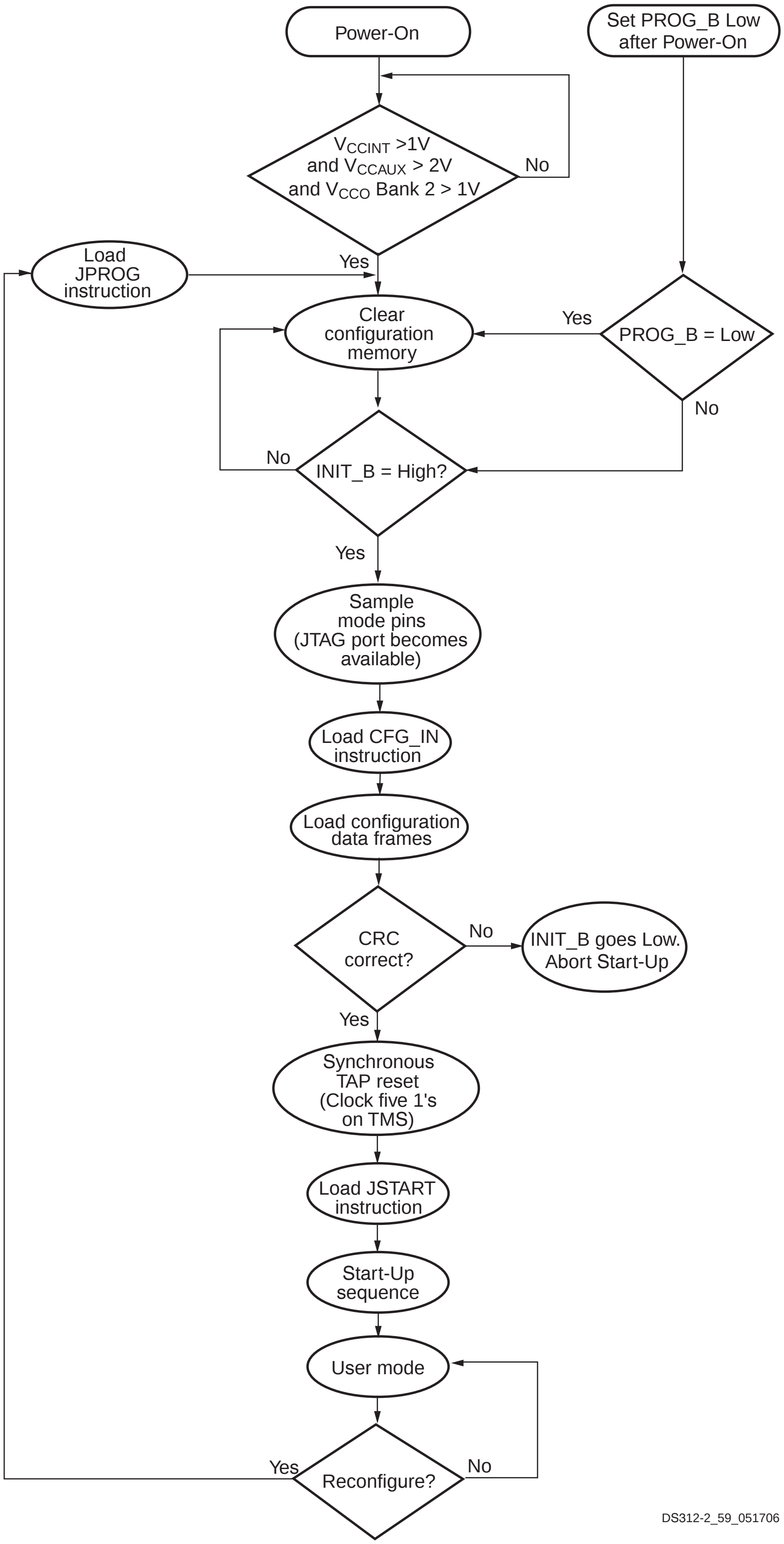

Figure 69: **Boundary-Scan Configuration Flow Diagram**

Start-Up

At the end of configuration, the FPGA automatically pulses the Global Set/Reset (GSR) signal, placing all flip-flops in a known state. After configuration completes, the FPGA switches over to the user application loaded into the FPGA. The sequence and timing of how the FPGA switches over is programmable as is the clock source controlling the sequence.

The default start-up sequence appears in Figure 70, where the Global Three-State signal (GTS) is released one clock cycle after DONE goes High. This sequence allows the DONE signal to enable or disable any external logic used during configuration before the user application in the FPGA starts driving output signals. One clock cycle later, the Global Write Enable (GWE) signal is released. This allows signals to propagate within the FPGA before any clocked storage elements such as flip-flops and block ROM are enabled.

The function of the dual-purpose I/O pins, such as M[2:0], VS[2:0], HSWAP, and A[23:0], also changes when the DONE pin goes High. When DONE is High, these pins become user I/Os. Like all user-I/O pins, GTS controls when the dual-purpose pins can drive out.

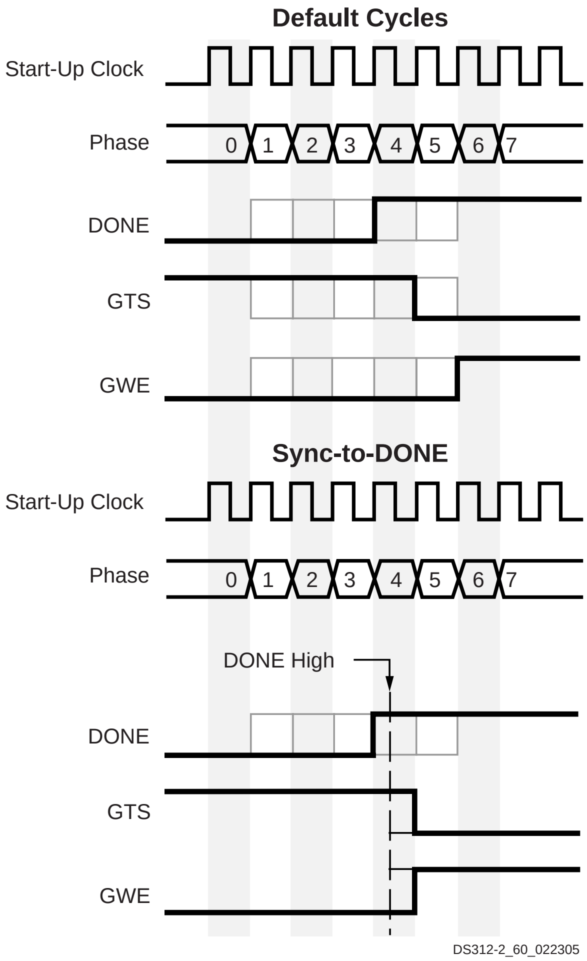

Figure 70: **Default Start-Up Sequence**

The relative timing of configuration events is programmed via the Bitstream Generator (BitGen) options in the Xilinx development software. For example, the GTS and GWE events can be programmed to wait for all the DONE pins to High on all the devices in a multiple-FPGA daisy-chain, forcing the FPGAs to start synchronously. Similarly, the start-up sequence can be paused at any stage, waiting for selected DCMs to lock to their respective input clock signals. See also **Stabilizing DCM Clocks Before User Mode**.

By default, the start-up sequence is synchronized to CCLK. Alternatively, the start-up sequence can be synchronized to a user-specified clock from within the FPGA application using the STARTUP_SPARTAN3E library primitive and by setting the ***StartupClk*** bitstream generator option. The FPGA application can optionally assert the GSR and GTS signals via the STARTUP_SPARTAN3E primitive. For JTAG configuration, the start-up sequence can be synchronized to the TCK clock input.

Readback

FPGA configuration data can be read back using either the Slave Parallel or JTAG mode. This function is disabled if the Bitstream Generator ***Security*** option is set to either ***Level1*** or ***Level2***.

Along with the configuration data, it is possible to read back the contents of all registers, distributed RAM, and block RAM resources.

To synchronously control when register values are captured for readback, use the CAPTURE_SPARTAN3 library primitive, which applies for both Spartan-3 and Spartan-3E FPGA families.

The Readback feature is available in most Spartan-3E FPGA product options, as indicated in Table 67. The Readback feature is not available in the XC3S1200E and XC3S1600E FPGAs when using the -4 speed grade in the Commercial temperature grade. If Readback is required for these devices, upgrade to either the Industrial temperature grade version or the -5 speed grade.

The Xilinx iMPACT programming software uses the Readback feature for its optional Verify and Readback operations. The Xilinx ChipScope™ software does not use Readback.

Table 67: **Readback Support in Spartan-3E FPGAs**

Temperature Range	**Commercial**		**Industrial**
Speed Grade	**-4**	**-5**	**-4**
XC3S100E	Yes	Yes	Yes
XC3S250E	Yes	Yes	Yes
XC3S500E	Yes	Yes	Yes
XC3S1200E	No	Yes	Yes
XC3S1600E	No	Yes	Yes

Bitstream Generator (BitGen) Options

Various Spartan-3E FPGA functions are controlled by specific bits in the configuration bitstream image. These values are specified when creating the bitstream image with the Bitstream Generator (BitGen) software.

Table 68 provides a list of all BitGen options for Spartan-3E FPGAs.

Table 68: **Spartan-3E FPGA Bitstream Generator (BitGen) Options**

Option Name	**Pins/Function Affected**	**Values (*default*)**	**Description**
ConfigRate	CCLK, Configuration	***1***, 3, 6, 12, 25, 50	Sets the approximate frequency, in MHz, of the internal oscillator using for Master Serial, SPI, and BPI configuration modes. The internal oscillator powers up at its lowest frequency, and the new setting is loaded as part of the configuration bitstream. The software default value is 1 (~1.5 MHz) starting with ISE 8.1, Service Pack 1.
StartupClk	Configuration, Startup	***Cclk***	***Default.*** The CCLK signal (internally or externally generated) controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See **Start-Up**.
		UserClk	A clock signal from within the FPGA application controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See **Start-Up**. The FPGA application supplies the user clock on the CLK pin on the STARTUP_SPARTAN3E primitive.
		Jtag	The JTAG TCK input controls the startup sequence when the FPGA transitions from the configuration mode to the user mode. See **Start-Up**.

Table 68: **Spartan-3E FPGA Bitstream Generator (BitGen) Options *(Continued)***

Option Name	Pins/Function Affected	Values (***default***)	Description
UnusedPin	Unused I/O Pins	***Pulldown***	***Default.*** All unused I/O pins and input-only pins have a pull-down resistor to GND.
		Pullup	All unused I/O pins and input-only pins have a pull-up resistor to the VCCO_# supply for its associated I/O bank.
		Pullnone	All unused I/O pins and input-only pins are left floating (Hi-Z, high-impedance, three-state). Use external pull-up or pull-down resistors or logic to apply a valid signal level.
DONE_cycle	DONE pin, Configuration Startup	1, 2, 3, ***4***, 5, 6	Selects the Configuration Startup phase that activates the FPGA's DONE pin. See **Start-Up**.
GWE_cycle	All flip-flops, LUT RAMs, and SRL16 shift registers, Block RAM, Configuration Startup	1, 2, 3, 4, 5, ***6***	Selects the Configuration Startup phase that asserts the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). It also enables block RAM read and write operations. See **Start-Up**.
		Done	Waits for the DONE pin input to go High before asserting the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). Block RAM read and write operations are enabled at this time.
		Keep	Retains the current GWE_cycle setting for partial reconfiguration applications.
GTS_cycle	All I/O pins, Configuration	1, 2, 3, 4, ***5***, 6	Selects the Configuration Startup phase that releases the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point. See **Start-Up**.
		Done	Waits for the DONE pin input to go High before releasing the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point.
		Keep	Retains the current GTS_cycle setting for partial reconfiguration applications.
LCK_cycle	DCMs, Configuration Startup	***NoWait***	The FPGA does not wait for selected DCMs to lock before completing configuration.
		0, 1, 2, 3, 4, 5, 6	If one or more DCMs in the design have the STARTUP_WAIT attribute set to TRUE, the FPGA waits for such DCMs to acquire their respective input clock and assert their LOCKED output. This setting selects the Configuration Startup phase where the FPGA waits for the DCMs to lock.
DonePin	DONE pin	***Pullup***	Internally connects a pull-up resistor between DONE pin and V_{CCAUX}. An external 330 Ω pull-up resistor to V_{CCAUX} is still recommended.
		Pullnone	No internal pull-up resistor on DONE pin. An external 330 Ω pull-up resistor to V_{CCAUX} is required.
DriveDone	DONE pin	***No***	When configuration completes, the DONE pin stops driving Low and relies on an external 330 Ω pull-up resistor to V_{CCAUX} for a valid logic High.
		Yes	When configuration completes, the DONE pin actively drives High. When using this option, an external pull-up resistor is no longer required. Only one device in an FPGA daisy-chain should use this setting.
DonePipe	DONE pin	***No***	The input path from DONE pin input back to the Startup sequencer is not pipelined.
		Yes	This option adds a pipeline register stage between the DONE pin input and the Startup sequencer. Used for high-speed daisy-chain configurations when DONE cannot rise in a single CCLK cycle. Releases GWE and GTS signals on the first rising edge of StartupClk after the DONE pin input goes High.

Table 68: **Spartan-3E FPGA Bitstream Generator (BitGen) Options *(Continued)***

Option Name	Pins/Function Affected	Values (***default***)	Description
ProgPin	PROG_B pin	***Pullup***	Internally connects a pull-up resistor or between PROG_B pin and V_{CCAUX}. An external 4.7 kΩ pull-up resistor to V_{CCAUX} is still recommended.
		Pullnone	No internal pull-up resistor on PROG_B pin. An external 4.7 kΩ pull-up resistor to V_{CCAUX} is required.
TckPin	JTAG TCK pin	***Pullup***	Internally connects a pull-up resistor between JTAG TCK pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TCK pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TCK pin.
TdiPin	JTAG TDI pin	***Pullup***	Internally connects a pull-up resistor between JTAG TDI pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TDI pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TDI pin.
TdoPin	JTAG TDO pin	***Pullup***	Internally connects a pull-up resistor between JTAG TDO pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TDO pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TDO pin.
TmsPin	JTAG TMS pin	***Pullup***	Internally connects a pull-up resistor between JTAG TMS pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TMS pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TMS pin.
UserID	JTAG User ID register	User string	The 32-bit JTAG User ID register value is loaded during configuration. The default value is all ones, 0xFFFF_FFFF hexadecimal. To specify another value, enter an 8-character hexadecimal value.
Security	JTAG, SelectMAP, Readback, Partial reconfiguration	***None***	Readback and limited partial reconfiguration are available via the JTAG port or via the SelectMAP interface, if the ***Persist*** option is set to ***Yes***.
		Level1	Readback function is disabled. Limited partial reconfiguration is still available via the JTAG port or via the SelectMAP interface, if the ***Persist*** option is set to ***Yes***.
		Level2	Readback function is disabled. Limited partial reconfiguration is disabled.
CRC	Configuration	**Enable**	***Default.*** Enable CRC checking on the FPGA bitstream. If error detected, FPGA asserts INIT_B Low and DONE pin stays Low.
		Disable	Turn off CRC checking.
Persist	SelectMAP interface pins, BPI mode, Slave mode, Configuration	***No***	All BPI and Slave mode configuration pins are available as user-I/O after configuration.
		Yes	This option is required for Readback and partial reconfiguration using the SelectMAP interface. The SelectMAP interface pins (see **Slave Parallel Mode**) are reserved after configuration and are not available as user-I/O.

Powering Spartan-3E FPGAs

Voltage Supplies

Like Spartan-3 FPGAs, Spartan-3E FPGAs have multiple voltage supply inputs, as shown in Table 69. There are two supply inputs for internal logic functions, V_{CCINT} and V_{CCAUX}. Each of the four I/O banks has a separate V_{CCO} supply input that powers the output buffers within the associated I/O bank. All of the V_{CCO} connections to a specific I/O bank must be connected and must connect to the same voltage.

Table 69: **Spartan-3E Voltage Supplies**

Supply Input	Description	Nominal Supply Voltage
V_{CCINT}	Internal core supply voltage. Supplies all internal logic functions, such as CLBs, block RAM, and multipliers. Input to Power-On Reset (POR) circuit.	1.2V
V_{CCAUX}	Auxiliary supply voltage. Supplies Digital Clock Managers (DCMs), differential drivers, dedicated configuration pins, JTAG interface. Input to Power-On Reset (POR) circuit.	2.5V
VCCO_0	Supplies the output buffers in I/O Bank 0, the bank along the top edge of the FPGA.	Selectable, 3.3V, 3.0V, 2.5V, 1.8, 1.5V, or 1.2V
VCCO_1	Supplies the output buffers in I/O Bank 1, the bank along the right edge of the FPGA. In **Byte-Wide Peripheral Interface (BPI) Parallel Flash Mode**, connects to the same voltage as the Flash PROM.	Selectable, 3.3V, 3.0V, 2.5V, 1.8, 1.5V, or 1.2V
VCCO_2	Supplies the output buffers in I/O Bank 2, the bank along the bottom edge of the FPGA. Connects to the same voltage as the FPGA configuration source. Input to Power-On Reset (POR) circuit.	Selectable, 3.3V, 3.0V, 2.5V, 1.8, 1.5V, or 1.2V
VCCO_3	Supplies the output buffers in I/O Bank 3, the bank along the left edge of the FPGA.	Selectable, 3.3V, 3.0V, 2.5V, 1.8, 1.5V, or 1.2V

In a 3.3V-only application, all four V_{CCO} supplies connect to 3.3V. However, Spartan-3E FPGAs provide the ability to bridge between different I/O voltages and standards by applying different voltages to the V_{CCO} inputs of different banks. Refer to **I/O Banking Rules** for which I/O standards can be intermixed within a single I/O bank.

Each I/O bank also has an separate, optional input voltage reference supply, called V_{REF}. If the I/O bank includes an I/O standard that requires a voltage reference such as HSTL or SSTL, then all V_{REF} pins within the I/O bank must be connected to the same voltage.

Voltage Regulators

Various power supply manufacturers offer complete power solutions for Xilinx FPGAs including some with integrated three-rail regulators specifically designed for Spartan-3 and Spartan-3E FPGAs. The Xilinx Power Corner website provides links to vendor solution guides and Xilinx power estimation and analysis tools.

Power Distribution System (PDS) Design and Decoupling/Bypass Capacitors

Good power distribution system (PDS) design is important for all FPGA designs, but especially so for high performance applications, greater than 100 MHz. Proper design results in better overall performance, lower clock and DCM jitter, and a generally more robust system. Before designing the printed circuit board (PCB) for the FPGA design, please review XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

Power-On Behavior

Spartan-3E FPGAs have a built-in Power-On Reset (POR) circuit that monitors the three power rails required to successfully configure the FPGA. At power-up, the POR circuit holds the FPGA in a reset state until the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supplies reach their respective input threshold levels (see Table 73 in Module 3). After all three supplies reach their respective thresholds, the POR reset is released and the FPGA begins its configuration process.

Supply Sequencing

Because the three FPGA supply inputs must be valid to release the POR reset and can be supplied in any order, there are no FPGA-specific voltage sequencing requirements. Applying the FPGA's V_{CCAUX} supply before the V_{CCINT} supply uses the least I_{CCINT} current.

Although the FPGA has no specific voltage sequence requirements, be sure to consider any potential sequencing requirement of the configuration device attached to the FPGA, such as an SPI serial Flash PROM, a parallel NOR Flash PROM, or a microcontroller. For example, Flash PROMs have a minimum time requirement before the PROM can be selected and this must be considered if the 3.3V supply is the last in the sequence. See **Power-On Precautions if 3.3V Supply is Last in Sequence** for more details.

When all three supplies are valid, the minimum current required to power-on the FPGA equals the worst-case quiescent current, specified in Table 78. Spartan-3E FPGAs do not require Power-On Surge (POS) current to successfully configure.

Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}

If the V_{CCINT} supply is applied before the V_{CCAUX} supply, the FPGA might draw a surplus I_{CCINT} current in addition to the I_{CCINT} quiescent current levels specified in Table 78, page 120. The momentary additional I_{CCINT} surplus current might be a few hundred milliamperes under nominal conditions, significantly less than the instantaneous current consumed by the bypass capacitors at power-on. However, the surplus current immediately disappears when the V_{CCAUX} supply is applied, and, in response, the FPGA's I_{CCINT} quiescent current demand drops to the levels specified in Table 78. The FPGA does not use or require the surplus current to successfully power-on and configure. If applying V_{CCINT} before V_{CCAUX}, ensure that the regulator does not have a foldback feature that could inadvertently shut down in the presence of the surplus current.

Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents, as specified in Table 75.

If, after configuration, the V_{CCAUX} or V_{CCINT} supply drops below its data retention voltage, the current device configuration must be cleared using one of the following methods:

- Force the V_{CCAUX} or V_{CCINT} supply voltage below the minimum Power On Reset (POR) voltage threshold (Table 73).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_2 supply after configuration. Consequently, dropping the VCCO_2 voltage does not reset the device by triggering a Power-On Reset (POR) event.

No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3E FPGA circuitry is fully static and does not employ internal charge pumps.

The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist*=*Yes***.

Production Stepping

The Spartan-3E FPGA family uses production stepping to indicate improved capabilities or enhanced features.

All devices ordered using the standard part number support Stepping 0 functionality and performance. Later steppings are, by definition, a functional superset of any previous stepping. Furthermore, configuration bitstreams generated for any stepping are compatible with later steppings.

When a new stepping is released to production, Xilinx will ship either the previous or new stepping version for a time before shipping only the new version. Designs operating on the current stepping function similarly on a later stepping level.

Differences Between Steppings

Table 70 summarizes the feature and performance differences between the current Stepping 0 devices and the planned Stepping 1 devices. The features and performance for Stepping 1 devices are target specifications pending final characterization.

Table 70: **Differences between Spartan-3E Production Stepping Levels**

	Stepping 0	Stepping 1
Production status	Production	Production starting March 2006
JTAG ID code	Different revision fields. See Table 66.	
DCM DLL maximum input frequency	90 MHz	240 MHz (–4 speed grade) 275 MHz (–5 speed grade)
DCM DFS output frequency range(s)	Split ranges at 5 – 90 MHz and 220 – 307 MHz	Continuous range: 5 – 311 MHz (–4) 5 – 333 MHz (–5)
Supports multi-FPGA daisy-chain configurations from SPI Flash	No, single FPGA only	Yes
JTAG configuration supported when FPGA in BPI mode with a valid image in the attached parallel NOR Flash PROM	No(1)	Yes
JTAG EXTEST, INTEST, SAMPLE support	Yes: XC3S100E, XC3S250E, XC3S500E No(2): XC3S1200E, XC3S1600E	Yes All Devices

Notes:

1. Workarounds exist. See **Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration**.
2. JTAG BYPASS and JTAG configuration are supported

Ordering a Later Stepping

Spartan-3E FPGAs ordered using the standard part number always support the Stepping 0 feature set. To order only the later stepping, append an “S#” suffix to the standard ordering code, where ‘#’ is the stepping number, as indicated in Table 71. Beginning with Stepping 1 and later, the stepping level is marked on the device using a single number character, as shown in Figure 2, Figure 3, and Figure 4 in Module 1. Stepping 0 devices are represented with either a ‘0’ mark or no mark. See **Ordering Information**, page 7 in Module 1 for additional information.

Table 71: **Spartan-3E Stepping Levels**

Stepping Number	Suffix Code	Status
0	None	Production
1	S1	Planned

Software Version Requirements

Production Spartan-3E applications must be processed using the Xilinx ISE 8.1i, Service Pack 3 or later development software, using the v1.21 or later speed files. The ISE 8.1i software implements critical bitstream generator updates.

For additional information on Spartan-3E development software and known issues, see the following Answer Record:

- **Xilinx Answer #22253**
  www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=22253

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Updated Figure 46. Modified title on Table 39 and Table 44.
11/23/05	2.0	Updated values of **On-Chip Differential Termination** resistors. Updated Table 7. Updated configuration bitstream sizes for XC3S250E through XC3S1600E in Table 44, Table 50, Table 56, and Table 59. Added **DLL Performance Differences Between Steppings**. Added **Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration**. Added Stepping 0 limitations when **Daisy-Chaining** in SPI configuration mode. Added **Multiplier/Block RAM Interaction** section. Updated **Digital Clock Managers (DCMs)** section, especially **Phase Shifter (PS)** portion. Corrected and enhanced the clock infrastructure diagram in Figure 46 and Table 41. Added **CCLK Design Considerations** section. Added **Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins** section. Added Spansion, Winbond, and Macronix to list of SPI Flash vendors in Table 52 and Table 55. Clarified that SPI mode configuration supports Atmel 'C'- and 'D'-series DataFlash. Updated the **Programming Support** section for SPI Flash PROMs. Added **Power-On Precautions if PROM Supply is Last in Sequence**, **Compatible Flash Families**, and **BPI Mode Interaction with Right and Bottom Edge Global Clock Inputs** sections to BPI configuration mode topic. Updated and amplified **Powering Spartan-3E FPGAs** section. Added **Production Stepping** section.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Updated **Input Delay Functions** and Figure 6. Added clarification that Input-only pins also have **Pull-Up and Pull-Down Resistors**. Added design note about address setup and hold requirements to **Block RAM**. Added warning message about software differences between ISE 8.1i, Service Pack 3 and earlier software to **FIXED Phase Shift Mode** and **VARIABLE Phase Shift Mode**. Added message about using GCLK1 in **DLL Clock Input Connections** and **Clock Inputs**. Updated Figure 46. Added additional information on HSWAP behavior to **Pin Behavior During Configuration**. Highlighted which pins have configuration pull-up resistors unaffected by HSWAP in Table 45. Updated bitstream image sizes for the XC3S1200E and XC3S1600E in Table 44, Table 50, Table 56, and Table 59. Clarified that 'B'-series Atmel DataFlash SPI PROMs can be used in Commercial temperature range applications in Table 52 and Figure 55. Updated Figure 57. Updated **Dynamically Loading Multiple Configuration Images Using MultiBoot Option** section. Added design note about BPI daisy-chaining software support to BPI **Daisy-Chaining** section. Updated JTAG revision codes in Table 66. Added **No Internal Charge Pumps or Free-Running Oscillators**. Updated information on production stepping differences in Table 70. Updated **Software Version Requirements**.
04/10/06	3.1	Updated **JTAG User ID** information. Clarified Note 1, Figure 5. Clarified that Figure 46 shows electrical connectiving and corrected left- and right-edge DCM coordinates. Updated Table 30, Table 31, and Table 32 to show the specific clock line driven by the associated BUFGMUX primitive. Corrected the coordinate locations for the associated BUFGMUX primitives in Table 31 and Table 32. Updated Table 41 to show that the I0-input is the preferred connection to a BUFGMUX.
05/19/06	3.2	Made further clarifying changes to Figure 46, showing both direct inputs to BUFGMUX primitives and to DCMs. Added Atmel AT45DBxxxD-series DataFlash serial PROMs to Table 52. Added details that intermediate FPGAs in a BPI-mode, multi-FPGA configuration daisy-chain must be from either the Spartan-3E or the Virtex-5 FPGA families (see BPI **Daisy-Chaining**). Added **Using JTAG Interface to Communicate to a Configured FPGA Design**. Minor updates to Figure 68 and Figure 69. Clarified which Spartan-3E FPGA product options support the Readback feature, shown in Table 67.

Spartan-3E FPGA Family: DC and Switching Characteristics

DS312-3 (v3.2) May 19, 2006

Preliminary Product Specification

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan™-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 72: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 72: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.00	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	$V_{CCO} + 0.5^{(2)}$	V
$V_{IN}^{(2,3)}$	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.5	$V_{CCO} + 0.5^{(2)}$	V
	Voltage applied to all Dedicated pins		–0.5	$V_{CCAUX} + 0.5^{(3)}$	V
I_{IK}	Input clamp current per I/O pin	$-0.5\text{ V} < V_{IN} < (V_{CCO} + 0.5\text{ V})$	-	100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–2000	+2000	V
		Charged device model	–500	+500	V
		Machine model	–200	+200	V
T_J	Junction temperature		-	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. As a rule, the V_{IN} limits apply to both the DC and AC components of signals. Simple application solutions are available that show how to handle overshoot/undershoot as well as achieve PCI compliance. Refer to XAPP653: *Virtex™-II Pro and Spartan-3 3.3V PCI Reference Design* and XAPP659: *Using 3.3V I/O Guidelines in a Virtex-II Pro Design*.
2. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} rails do not turn on. Table 76 specifies the V_{CCO} range used to evaluate the maximum V_{IN} voltage.
3. Voltages beyond the minimum and maximum V_{IN} input voltage range are permissible provided that the I_{IK} input diode clamp diode rating is met. The absolute maximum voltage at the pin, V_{INX}, must never exceed 4.05V. Limiting the input voltage to below 4.05V avoids stressing the I/O oxide layer.
4. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 76 specifies the V_{CCAUX} range used to evaluate the maximum V_{IN} voltage. As long as the V_{IN} max specification is met, oxide stress is not possible.
5. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

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Power Supply Specifications

Table 73: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 74: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	50	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	50	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	50	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 75: **Supply Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include configuration data.

General Recommended Operating Conditions

Table 76: **General Recommended Operating Conditions**

Symbol	Description		Min	Nominal	Max	Units
T_J	Junction temperature	Commercial	0	-	85	°C
		Industrial	–40	-	100	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO}(1)	Output driver supply voltage		1.100	-	3.450	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V
T_{IN}	Input signal transition time(2)		-	-	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 79 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 81 lists that specific to the differential standards.
2. Measured between 10% and 90% V_{CCO}.

General DC Characteristics for I/O Pins

Table 77: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_L	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested	–10	-	+10	µA
I_{RPU}(2)	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = 0V, V_{CCO} = 3.3V	–0.36	-	–1.24	mA
		V_{IN} = 0V, V_{CCO} = 3.0V	–0.28	-	–1.20	mA
		V_{IN} = 0V, V_{CCO} = 2.5V	–0.22	-	–0.80	mA
		V_{IN} = 0V, V_{CCO} = 1.8V	–0.10	-	–0.42	mA
		V_{IN} = 0V, V_{CCO} = 1.5V	–0.06	-	–0.27	mA
		V_{IN} = 0V, V_{CCO} = 1.2V	–0.04	-	–0.22	mA
R_{PU}(2)	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2)	V_{IN} = 0V, V_{CCO} = 3.0V to 3.45V	2.4	-	10.8	kΩ
		V_{IN} = 0V, V_{CCO} = 2.3V to 2.7V	2.7	-	11.8	kΩ
		V_{IN} = 0V, V_{CCO} = 1.7V to 1.9V	4.3	-	20.2	kΩ
		V_{IN} = 0V, V_{CCO} =1.4V to 1.6V	5.0	-	25.9	kΩ
		V_{IN} = 0V, V_{CCO} = 1.14V to 1.26V	5.5	-	32.0	kΩ
I_{RPD}(2)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = V_{CCO}	0.10		0.75	mA
R_{PD}(2)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	V_{IN} = V_{CCO} = 3.0V to 3.45V	4.0	-	34.5	kΩ
		V_{IN} = V_{CCO} = 2.3V to 2.7V	3.0	-	27.0	kΩ
		V_{IN} = V_{CCO} = 1.7V to 1.9V	2.3	-	19.0	kΩ
		V_{IN} = V_{CCO} = 1.4V to 1.6V	1.8	-	16.0	kΩ
		V_{IN} = V_{CCO} = 1.14V to 1.26V	1.5	-	12.6	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels	–10	-	+10	µA
C_{IN}	Input capacitance	-	3	-	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	-	-	120	-	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 76.
2. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

Quiescent Current Requirements

Table 78: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical[2]	Commercial Maximum[2]	Industrial Maximum[2]	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S100E	8	60	80	mA
		XC3S250E	15	120	160	mA
		XC3S500E	25	165	210	mA
		XC3S1200E	50	400	500	mA
		XC3S1600E	65	560	700	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S100E	1.5	8	10	mA
		XC3S250E	1.5	8	10	mA
		XC3S500E	2	10	12	mA
		XC3S1200E	3	12	15	mA
		XC3S1600E	3	12	15	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S100E	8	25	28	mA
		XC3S250E	12	30	35	mA
		XC3S500E	18	40	45	mA
		XC3S1200E	35	65	75	mA
		XC3S1600E	45	80	90	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 76.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at ambient room temperature (T_A of 25°C at V_{CCINT} = 1.2 V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.45V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a “blank” configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements), measured quiescent current levels may be different than the values in the table.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3E Web Power Tool provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.

Single-Ended I/O Standards

Table 79: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(2)			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.45	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33(4)	3.0	3.3	3.45				0.8	2.0
LVCMOS25(4,5)	2.3	2.5	2.7				0.7	1.7
LVCMOS18(4)	1.65	1.8	1.95				0.38	0.8
LVCMOS15(4)	1.4	1.5	1.6				0.38	0.8
LVCMOS12(4)	1.1	1.2	1.3				0.38	0.8
PCI33_3(6)	-	3.0	-				0.9	1.5
PCI66_3(6)	-	3.0	-				0.9	1.5
PCIX(6)	-	3.0	-					
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	-	1.1	-	V_{REF} - 0.1	V_{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} - 0.125	V_{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.125	V_{REF} + 0.125

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. The V_{CCO} rails supply only output drivers, not input circuits.
3. For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 72.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) use the LVCMOS25 standard and draw power from the V_{CCAUX} rail (2.5V). The Dual-Purpose configuration pins use the LVCMOS25 standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For more information, see XAPP653: *Virtex-II Pro and Spartan-3 3.3V PCI Reference Design*.

Table 80: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL[3]	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVCMOS33[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVCMOS25[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVCMOS18[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
LVCMOS15[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS12[3]	2	2	–2	0.4	V_{CCO} - 0.4
PCI33_3[4]		1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCI66_3[4]		1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCIX		1.5	–0.5	10% V_{CCO}	90% V_{CCO}
HSTL_I_18		8	–8	0.4	V_{CCO} - 0.4
HSTL_III_18		24	–8	0.4	V_{CCO} - 0.4
SSTL18_I		6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL2_I		8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61

Notes:

1. The numbers in this table are based on the conditions set forth in Table 76 and Table 79.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} — the output current condition under which V_{OL} is tested
   I_{OH} — the output current condition under which V_{OH} is tested
   V_{OL} — the output voltage that indicates a Low logic level
   V_{OH} — the output voltage that indicates a High logic level
   V_{IL} — the input voltage that indicates a Low logic level
   V_{IH} — the input voltage that indicates a High logic level
   V_{CCO} — the supply voltage for output drivers
   V_{REF} — the reference voltage for setting the input switching threshold
   V_{TT} — the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
4. Tested according to the relevant PCI specifications. For more information, see XAPP653: *Virtex-II Pro and Spartan-3 3.3V PCI Reference Design*.

Differential I/O Standards

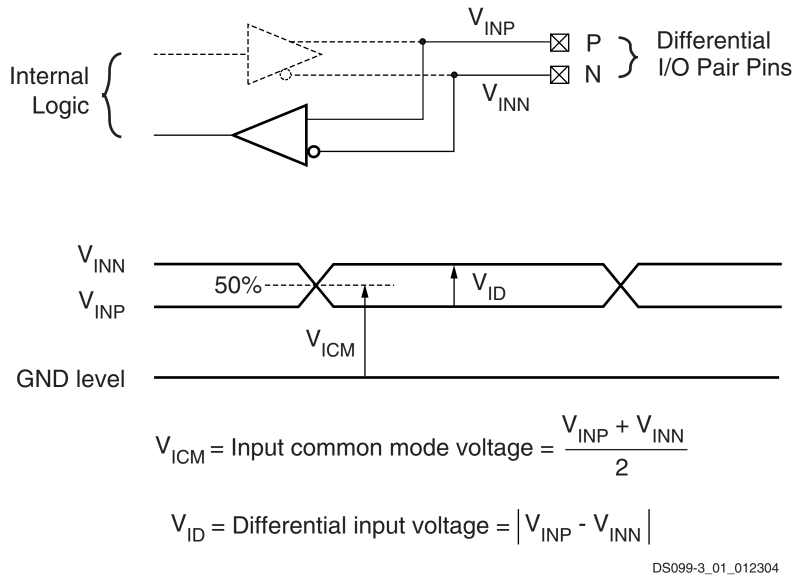

Figure 71: **Differential Input Voltages**

Table 81: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	**V_{CCO} for Drivers(1)**			**V_{ID}**			**V_{ICM}**			**V_{IH}**		**V_{IL}**	
	Min (V)	**Nom (V)**	**Max (V)**	**Min (mV)**	**Nom (mV)**	**Max (mV)**	**Min (V)**	**Nom (V)**	**Max (V)**	**Min (V)**	**Max (V)**	**Min (V)**	**Max (V)**
LVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20	-	-	-	-
BLVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20	-	-	-	-
MINI_LVDS_25	2.375	2.50	2.625	200	-	600	0.30	-	2.2				
LVPECL_25(2)	Inputs Only			100	800	1000	0.3	1.2	2.2	0.8	2.0	0.5	1.7
RSDS_25	2.375	2.50	2.625	100	200	-	0.3	1.20	1.4	-	-	-	-
DIFF_HSTL_I_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1	-	-	-	-
DIFF_HSTL_III_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1	-	-	-	-
DIFF_SSTL18_I	1.7	1.8	1.9	100	-	-	0.7	-	1.1	-	-	-	-
DIFF_SSTL2_I	2.3	2.5	2.7	100	-	-	1.0	-	1.5	-	-	-	-

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.

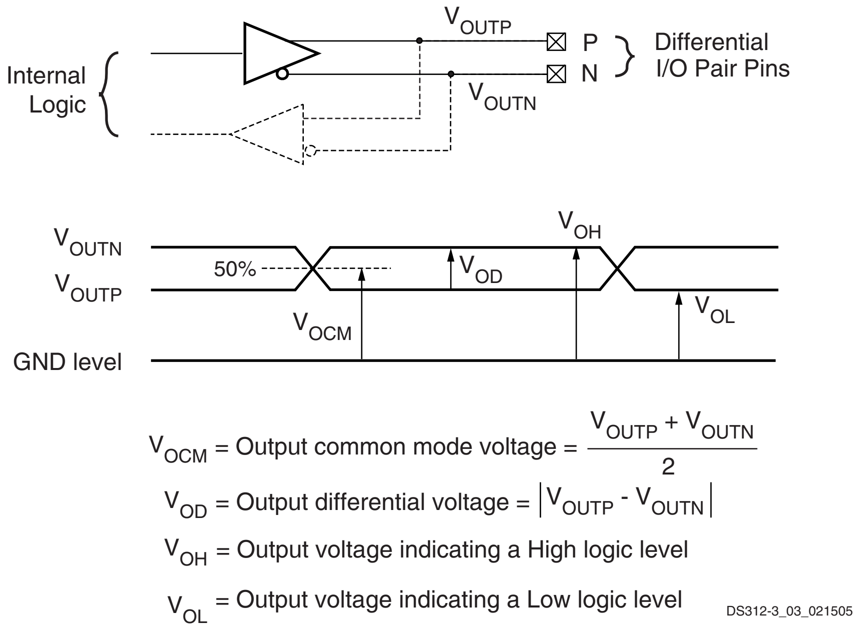

Figure 72: **Differential Output Voltages**

Table 82: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			ΔV_{OD}		V_{OCM}			ΔV_{OCM}		V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)
LVDS_25	250	350	450	-	-	1.125	-	1.375	-	-	1.25	1.25
BLVDS_25	250	350	450	-	-	-	1.20	-	-	-	-	-
MINI_LVDS_25	300	-	600	-	50	1.0	-	1.4	-	50	1.25	1.15
RSDS_25	100	-	400	-	-	1.1	-	1.4	-	-	1.35	1.15
DIFF_HSTL_I_18	-	-	-	-	-	-	-	-	-	-	$V_{CCO} – 0.4$	0.4
DIFF_HSTL_III_18	-	-	-	-	-	-	-	-	-	-	$V_{CCO} – 0.4$	0.4
DIFF_SSTL18_I	-	-	-	-	-	-	-	-	-	-	$V_{TT} + 0.475$	$V_{TT} – 0.475$
DIFF_SSTL2_I	-	-	-	-	-	-	-	-	-	-	$V_{TT} + 0.61$	$V_{TT} – 0.61$

Notes:

1. The numbers in this table are based on the conditions set forth in Table 76 and Table 81.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
3. At any given time, no more than two of the following differential output standards may be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25

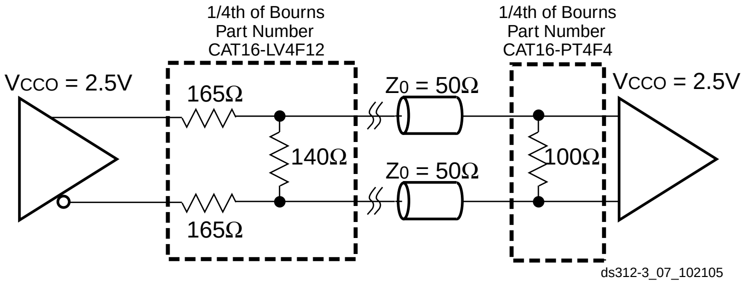

Figure 73: **External Termination Resistors for BLVDS I/Os**

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 83. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Production designs require the Xilinx ISE 8.1i, Service Pack 3 or later development software and the v1.21 or later speed files, indicated in Table 83.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan™-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Some specifications list different values for one or more device Steppings, indicated by the device top marking.

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.21), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 83. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 83: **Spartan-3E v1.21 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			–4, –5
XC3S250E			–4, –5
XC3S500E			–4, –5
XC3S1200E			–4, –5
XC3S1600E			–4, –5

I/O Timing

Table 84: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	**XC3S100E**	2.66	2.79	ns
			XC3S250E	3.00	3.45	ns
			XC3S500E	3.01	3.46	ns
			XC3S1200E	3.01	3.46	ns
			XC3S1600E	3.00	3.45	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	**XC3S100E**	5.60	5.92	ns
			XC3S250E	4.91	5.43	ns
			XC3S500E	4.98	5.51	ns
			XC3S1200E	5.36	5.94	ns
			XC3S1600E	5.45	6.05	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 92 and are based on the operating conditions set forth in Table 76 and Table 79.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 88. If the latter is true, *add* the appropriate Output adjustment from Table 91.
3. DCM output jitter is included in all measurements.

Table 85: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Sychronous)**

Symbol	Description	Conditions	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	**XC3S100E**	2.65	2.98	ns
			XC3S250E	2.25	2.59	ns
			XC3S500E	2.25	2.59	ns
			XC3S1200E	2.25	2.58	ns
			XC3S1600E	2.25	2.59	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 5, without DCM	**XC3S100E**	5.80	6.69	ns
			XC3S250E	4.77	5.66	ns
			XC3S500E	5.73	6.61	ns
			XC3S1200E	4.60	5.46	ns
			XC3S1600E	4.52	5.38	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	**XC3S100E**	–0.48	–0.43	ns
			XC3S250E	0.12	0.14	ns
			XC3S500E	0.13	0.14	ns
			XC3S1200E	0.13	0.15	ns
			XC3S1600E	0.12	0.14	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 5, without DCM	**XC3S100E**	–0.29	–0.24	ns
			XC3S250E	–0.72	–0.67	ns
			XC3S500E	–0.65	–0.60	ns
			XC3S1200E	–0.28	–0.23	ns
			XC3S1600E	–0.18	–0.13	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 92 and are based on the operating conditions set forth in Table 76 and Table 79.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 88. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 88. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 86: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0	All	1.84	2.12	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 5	All	7.49	8.61	ns
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0	All	–0.70	–0.70	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 5	All	–3.91	–3.91	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB		All	1.00	1.15	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 92 and are based on the operating conditions set forth in Table 76 and Table 79.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 88.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 88. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 87: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = 0	All	1.96	2.25	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = 5	All	7.03	8.08	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 92 and are based on the operating conditions set forth in Table 76 and Table 79.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 88.

Table 88: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below Speed Grade -5	Add the Adjustment Below Speed Grade -4	Units
Single-Ended Standards			
LVTTL	0.42	0.43	ns
LVCMOS33	0.42	0.43	ns
LVCMOS25	0	0	ns
LVCMOS18	0.96	0.98	ns
LVCMOS15	0.62	0.63	ns
LVCMOS12	0.26	0.27	ns
PCI33_3	0.41	0.42	ns
PCI66_3	0.41	0.42	ns
PCIX	0.22	0.22	ns
HSTL_I_18	0.12	0.12	ns
HSTL_III_18	0.17	0.17	ns
SSTL18_I	0.30	0.30	ns
SSTL2_I	0.15	0.15	ns

Table 88: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below Speed Grade -5	Add the Adjustment Below Speed Grade -4	Units
Differential Standards			
LVDS_25	0.48	0.49	ns
BLVDS_25	0.39	0.39	ns
MINI_LVDS_25	0.48	0.49	ns
LVPECL_25	0.27(3)	0.27(3)	ns
RSDS_25	0.48	0.49	ns
DIFF_HSTL_I_18	0.48	0.49	ns
DIFF_HSTL_III_18	0.48	0.49	ns
DIFF_SSTL18_I	0.30	0.30	ns
DIFF_SSTL2_I	0.32(3)	0.32(3)	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 92 and are based on the operating conditions set forth in Table 76, Table 79, and Table 81.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.
3. This value supersedes the value in the v1.21 speed file.

Table 89: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	**All**	2.18	2.50	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	**All**	2.24	2.58	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin			2.32	2.67	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	**All**	3.27	3.76	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3E primitive to setting/resetting data at the Output pin			8.40	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 92 and are based on the operating conditions set forth in Table 76 and Table 79.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 91.

Table 90: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.49	1.71	ns
T_{IOCKON}(2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	2.70	3.10	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3E primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	8.52	9.79	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	2.20	2.53	ns
T_{IOSRON}(2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.41	3.92	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 92 and are based on the operating conditions set forth in Table 76 and Table 79.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 91.

Table 91: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTL	Slow	2 mA	5.20	5.41	ns
		4 mA	2.32	2.41	ns
		6 mA	1.83	1.90	ns
		8 mA	0.64	0.67	ns
		12 mA	0.68	0.70	ns
		16 mA	0.41	0.43	ns
	Fast	2 mA	4.80	5.00	ns
		4 mA	1.88	1.96	ns
		6 mA	1.39	1.45	ns
		8 mA	0.32	0.34	ns
		12 mA	0.28	0.30	ns
		16 mA	0.28	0.30	ns
LVCMOS33	Slow	2 mA	5.08	5.29	ns
		4 mA	1.82	1.89	ns
		6 mA	1.00	1.04	ns
		8 mA	0.66	0.69	ns
		12 mA	0.40	0.42	ns
		16 mA	0.41	0.43	ns
	Fast	2 mA	4.68	4.87	ns
		4 mA	1.46	1.52	ns
		6 mA	0.38	0.39	ns
		8 mA	0.33	0.34	ns
		12 mA	0.28	0.30	ns
		16 mA	0.28	0.30	ns
LVCMOS25	Slow	2 mA	4.04	4.21	ns
		4 mA	2.17	2.26	ns
		6 mA	1.46	1.52	ns
		8 mA	1.04	1.08	ns
		12 mA	0.65	0.68	ns
	Fast	2 mA	3.53	3.67	ns
		4 mA	1.65	1.72	ns
		6 mA	0.44	0.46	ns
		8 mA	0.20	0.21	ns
		12 mA	0	0	ns
LVCMOS18	Slow	2 mA	5.03	5.24	ns
		4 mA	3.08	3.21	ns
		6 mA	2.39	2.49	ns
		8 mA	1.83	1.90	ns
	Fast	2 mA	3.98	4.15	ns
		4 mA	2.04	2.13	ns
		6 mA	1.09	1.14	ns
		8 mA	0.72	0.75	ns
LVCMOS15	Slow	2 mA	4.49	4.68	ns
		4 mA	3.81	3.97	ns
		6 mA	2.99	3.11	ns
	Fast	2 mA	3.25	3.38	ns
		4 mA	2.59	2.70	ns
		6 mA	1.47	1.53	ns
LVCMOS12	Slow	2 mA	6.36	6.63	ns
	Fast	2 mA	4.26	4.44	ns
HSTL_I_18			0.33	0.34	ns
HSTL_III_18			0.53	0.55	ns
PCI33_3			0.44	0.46	ns
PCI66_3			0.44	0.46	ns
PCIX			0.82	0.85	ns
SSTL18_I			0.24	0.25	ns
SSTL2_I			–0.20	–0.20	ns
Differential Standards					
LVDS_25			–0.55	–0.55	ns
BLVDS_25			0.04	0.04	ns
MINI_LVDS_25			–0.56	–0.56	ns
LVPECL_25			Input Only		ns
RSDS_25			–0.48	–0.48	ns
DIFF_HSTL_I_18			0.42(3)	0.42(3)	ns
DIFF_HSTL_III_18			0.53	0.55	ns
DIFF_SSTL18_I			0.40(3)	0.40(3)	ns
DIFF_SSTL2_I			0.44(3)	0.44(3)	ns

Notes:

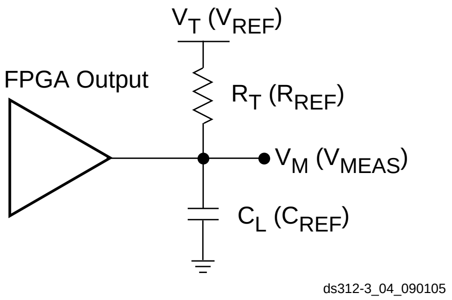
1. The numbers in this table are tested using the methodology presented in Table 92 and are based on the operating conditions set forth in Table 76, Table 79, and Table 81.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.
3. This value supersedes the value in the v1.21 speed file.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 92 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 74. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 74: **Output Test Setup**

Table 92: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCIX	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
Differential							
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}

Table 92: **Test Methods for Timing Measurement at I/Os *(Continued)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
DIFF_HSTL_I_18	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
DIFF_HSTL_III_18	1.1	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.8	V_{REF}
DIFF_SSTL18_I	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
DIFF_SSTL2_I	1.25	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.25	V_{REF}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1MW when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 92 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 74. Use parameter values V_T, R_T, and V_M from Table 92. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 91) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 93 and Table 94 provide the essential SSO guidelines. For each device/package combination, Table 93 provides the number of equivalent V_{CCO}/GND pairs. For each output signal standard and drive strength, Table 94 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 94 are categorized by package style. Multiply the appropriate numbers from Table 93 and Table 94 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 93 x Table 94

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. The results for chip-scale packaging (CP132) are better than quad-flat packaging but not as high as for ball grid array packaging. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 93: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	**Package Style *(including Pb-free)***							
	VQ100	**CP132**	**TQ144**	**PQ208**	**FT256**	**FG320**	**FG400**	**FG484**
XC3S100E	2	2	2	-	-	-	-	-
XC3S250E	2	2	2	3	4	-	-	-
XC3S500E	-	2	-	3	4	5	-	-
XC3S1200E	-	-	-	-	4	5	6	-
XC3S1600E	-	-	-	-	-	5	6	7

Table 94: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair**

Signal Standard (IOSTANDARD)			Package Type				
			VQ 100	TQ 144	PQ 208	CP 132	FT256, FG320, FG400, FG484
Single-Ended Standards							
LVTTL	Slow	2	34	20	19	52	60
		4	17	10	10	26	41
		6	17	10	7	26	29
		8	8	6	6	13	22
		12	8	6	5	13	13
		16	5	5	5	6	11
	Fast	2	17	17	17	26	34
		4	9	9	9	13	20
		6	7	7	7	13	15
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	5	5	5	5	9
LVCMOS33	Slow	2	34	20	20	52	76
		4	17	10	10	26	46
		6	17	10	7	26	27
		8	8	6	6	13	20
		12	8	6	5	13	13
		16	5	5	5	6	10
	Fast	2	17	17	17	26	44
		4	8	8	8	13	26
		6	8	6	6	13	16
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	8	8	5	5	8
LVCMOS25	Slow	2	28	16	16	42	76
		4	13	10	10	19	46
		6	13	7	7	19	33
		8	6	6	6	9	24
		12	6	6	6	9	18
	Fast	2	17	16	16	26	42
		4	9	9	9	13	20
		6	9	7	7	13	15
		8	6	6	6	6	13
		12	5	5	5	6	11
LVCMOS18	Slow	2	19	11	8	29	64
		4	13	7	6	19	34
		6	6	5	5	9	22
		8	6	4	4	9	18
	Fast	2	13	8	8	19	36
		4	8	5	5	13	21
		6	4	4	4	6	13
		8	4	4	4	6	10
LVCMOS15	Slow	2	16	10	10	19	55
		4	8	7	7	9	31
		6	6	5	5	9	18
	Fast	2	9	9	9	13	25
		4	7	7	7	7	16
		6	5	5	5	5	13
LVCMOS12	Slow	2	17	11	11	16	55
	Fast	2	10	10	10	10	31
PCI33_3			8	8	8	16	16
PCI66_3			8	8	8	13	13
PCIX			7	7	7	11	11
HSTL_I_18			10	10	10	16	17
HSTL_III_18			10	10	10	16	16
SSTL18_I			9	9	9	15	15
SSTL2_I			12	12	12	18	18
Differential Standards (Number of I/O Pairs or Channels)							
LVDS_25			6	6	6	12	20
BLVDS_25			4	4	4	4	4
MINI_LVDS_25			6	6	6	12	20
LVPECL_25			Input Only				
RSDS_25			6	6	6	12	20
DIFF_HSTL_I_18			5	5	5	8	8
DIFF_HSTL_IIII_18			5	5	5	8	8
DIFF_SSTL18_I			4	4	4	7	7
DIFF_SSTL2_I			6	6	6	9	8

Notes:

1. The numbers in this table are recommendations that assume sound board layout practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per V_{CCO} and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the VIL/VIH voltage limits forthe respective I/O standard.
2. The PQ208 results are based on physical measurements of a PQ208 package soldered to a typical printed circuit board. All other results are based on worst-case simulation and an interpolation of the PQ208 physical results.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

Configurable Logic Block (CLB) Timing

Table 95: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	-	0.52	-	0.60	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.46	-	0.52	-	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	0.32	-	0.36	-	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	-	0	-	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	-	0	-	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.70	-	0.80	-	ns
T_{CL}	The Low pulse width of the CLK signal	0.70	-	0.80	-	ns
F_{TOG}	Toggle frequency (for export control)	0	657	0	572	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	-	0.66	-	0.76	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.00	-	1.15	-	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 76.

Table 96: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	2.05	-	2.35	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.40	-	0.46	-	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	-	0.52	-	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.34	-	0.40	-	ns
Hold Times						
T_{DH}	Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	-	0.15	-	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	0	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Table 97: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	-	3.62	-	4.16	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.41	-	0.46	-	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.14	-	0.16	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 98: **Clock Distribution Switching Characteristics**

Description	Symbol	Minimum	Maximum Speed Grade		Units
			-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	-	1.46	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	-	0.55	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	0	333	311	MHz

18 x 18 Embedded Multiplier Timing

Table 99: **18 x 18 Embedded Multiplier Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T_{MULT}	Combinatorial multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	-	4.34(1)	-	4.88(1)	ns
Clock-to-Output Times						
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2)	-	0.98	-	1.10	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(2,4)	-	4.42	-	4.97	ns
Setup Times						
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)	3.54	-	3.98	-	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(4)	0.20	-	0.23	-	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(4)	0.35	-	0.39	-	ns
Hold Times						
$T_{MULCKID}$	Data hold time at the A and B inputs after the active transition at the CLK input	0	-	0	-	ns
Clock Frequency						
F_{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register(1)	0	270	0	240	MHz

Notes:

1. Combinatorial delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. The PREG register is typically used when inferring a single-stage multiplier.
4. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.

Block RAM Timing

Table 100: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	-	2.45	-	2.82	ns
Setup Times						
T_{BACK}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.33	-	0.38	-	ns
T_{BDCK}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.23	-	0.23	-	ns
T_{BECK}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.67	-	0.77	-	ns
T_{BWCK}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.09	-	1.26	-	ns
Hold Times						
T_{BCKA}	Hold time on the ADDR inputs after the active transition at the CLK input	0.12	-	0.14	-	ns
T_{BCKD}	Hold time on the DIN inputs after the active transition at the CLK input	0.12	-	0.13	-	ns
T_{BCKE}	Hold time on the EN input after the active transition at the CLK input	0	-	0	-	ns
T_{BCKW}	Hold time on the WE input after the active transition at the CLK input	0	-	0	-	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.39	-	1.59	-	ns
T_{BPWL}	Low pulse width of the CLK signal	1.39	-	1.59	-	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift-registers and circular buffers. Write-only or read-only performance is faster.	0	270	0	230	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 76.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 101 and Table 102) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 103 through Table 106) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 101 and Table 102.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Delay-Locked Loop (DLL)

Table 101: **Recommended Operating Conditions for the DLL**

Symbol		Description			Speed Grade				Units
					-5		-4		
					Min	Max	Min	Max	
Input Frequency Ranges									
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	5[2]	90[4]	5[2]	90[4]	MHz
				XC3S1200E[3]		200[4]		200[4]	MHz
			Stepping 1	All		275[4]		240[4]	MHz
Input Pulse Requirements									
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \le 150$ MHz		40%	60%	40%	60%	-
			$F_{CLKIN} > 150$ MHz		45%	55%	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation[4]									
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \le 150$ MHz		-	±300	-	±300	ps
CLKIN_CYC_JITT_DLL_HF			$F_{CLKIN} > 150$ MHz		-	±150	-	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input			-	±1	-	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input			-	±1	-	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 103.
3. Stepping 0 versions of XC3S250E and XC3S500E FPGAs, ordered under SCD4003, have the same performance as the Stepping 0 version of the XC3S1200E FPGA. The SCD4003 devices become obsolete when Stepping 1 versions become available.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock period by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
5. CLKIN input jitter beyond these limits might cause the DCM to lose lock.

Table 102: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges(2)								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	5	90	5	90	MHz
			XC3S1200E		200		200	MHz
		Stepping 1	All		275		240	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	5	90	5	90	MHz
			XC3S1200E		167		167	MHz
		Stepping 1	All		167		167	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	10	180	10	180	MHz
			XC3S1200E		333		311	MHz
		Stepping 1	All		333		311	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	0.3125	60	0.3125	60	MHz
			XC3S1200E		133		133	MHz
		Stepping 1	All		183		160	MHz
Output Clock Jitter(2,3,4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	-	±100	-	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			-	±[1% of CLKIN period + 150]	-	±[1% of CLKIN period + 150]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			-	±150	-	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			-	±[1% of CLKIN period + 200]	-	±[1% of CLKIN period + 200]	ps
Duty Cycle(4)								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKIN period + 400]	-	±[1% of CLKIN period + 400]	ps

Table 102: **Switching Characteristics for the DLL *(Continued)***

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Phase Alignment(5)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	-	±200	-	±200	ps
CLKOUT_PHASE_DLLstev	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		-	±[1% of CLKIN period + 100]	-	±[1% of CLKIN period + 100]	ps
		All others		-	±[1% of CLKIN period + 200]	-	±[1% of CLKIN period + 200]	ps
Lock Time								
LOCK_DLL(4)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	600	-	600	µs
Delay Lines								
DCM_DELAY_STEP	Finest delay resolution		All	20	40	20	40	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 76 and Table 101.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. ***Example:*** The data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.

Digital Frequency Synthesizer (DFS)

Table 103: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333	0.200	333	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \le 150$ MHz	-	±300	-	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	-	±150	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		-	±1	-	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 101.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Table 104: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges(2)								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs, low frequencies	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	5	90	5	90	MHz
CLKOUT_FREQ_FX_HF	Frequency for the CLKFX and CLKFX180 outputs, high frequencies			220	326	220	307	MHz
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	Stepping 0	XC3S1200E(2)	5	307	5	307	MHz
		Stepping 1	All		333		311	MHz
Output Clock Jitter(3,4)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs		All	See Note 4 below				ps
CLKOUT_PER_JITT_FX_35 (T_{J35})	Period jitter at the CLKFX and CLKFX180 outputs when CLKFX_MULTIPLY=7, CLKFX_DIVIDE=2		All in FG or CP packages		±[2% of CLKFX period + 400]		±[2% of CLKFX period + 400]	ps
Duty Cycle(5,6)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKFX period + 400]	-	±[1% of CLKFX period + 400]	ps
Phase Alignment(6)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±200	-	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±[1% of CLKFX period + 300]	-	±[1% of CLKFX period + 300]	ps

Table 104: **Switching Characteristics for the DFS *(Continued)***

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Lock Time								
LOCK_FX(3)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	450	-	450	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 76 and Table 103.
2. Stepping 0 devices, not specifically ordered under SCD4003, have both a Low and a High Frequency output range. Stepping 0 versions of the XC3S1200E, Stepping 0 devices ordered under SCD4003, and all Stepping 1 devices support a continuous, broad output frequency range.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Use the Virtex-II Jitter Calculator at http://www.xilinx.com/applications/web_ds_v2/jitter_calc.htm.or the jitter calculator included in Clock Wizard/DCM Wizard. Output jitter includes 150 ps of input clock jitter.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include 1% of the CLKFX output period or 0.01 UI. ***Example:*** The data sheet specifies a maximum jitter of "±[1% of CLKFX period + 300]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 300 ps] = ±400 ps.

Phase Shifter (PS)

Table 105: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 106: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description		Units
Phase Shifting Range			
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	±[INTEGER(20 • (T_{CLKIN} – 3 ns))]	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MIN]	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MAX]	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 76 and Table 105.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 102.

Miscellaneous DCM Timing

Table 107: **Miscellaneous DCM Timing**

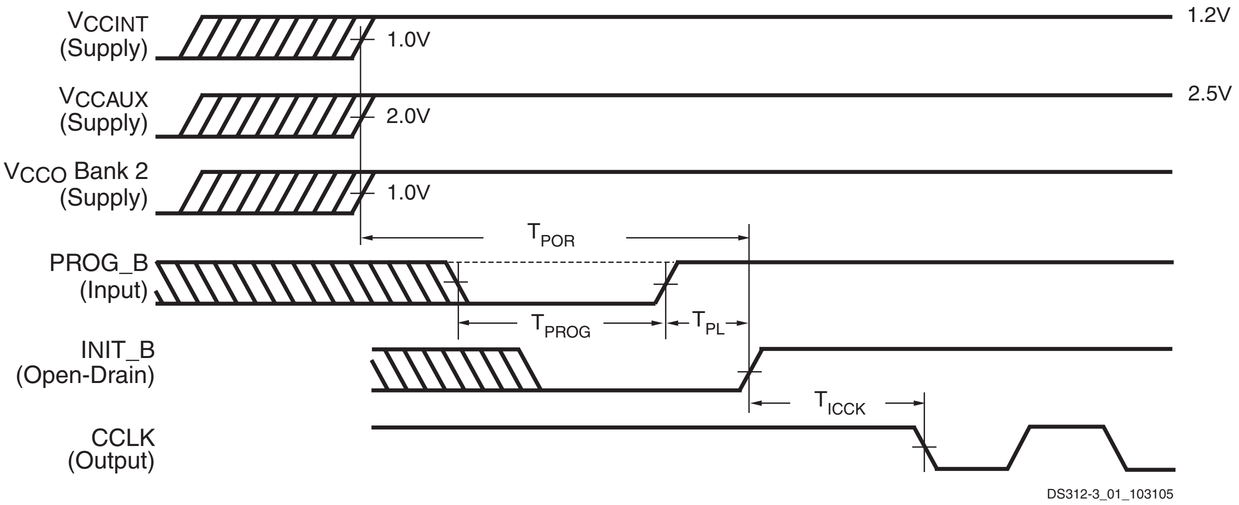
Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
		N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes
		N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specfication.This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 75: **Waveforms for Power-On and the Beginning of Configuration**

Table 108: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S100E	-	5	ms
		XC3S250E	-	5	ms
		XC3S500E	-	5	ms
		XC3S1200E	-	5	ms
		XC3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S100E	-	0.5	ms
		XC3S250E	-	0.5	ms
		XC3S500E	-	1	ms
		XC3S1200E	-	2	ms
		XC3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 76. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Configuration Clock (CCLK) Characteristics

Table 109: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	570	1,250	ns
			Industrial	485		ns
T_{CCLK3}		3	Commercial	285	625	ns
			Industrial	242		ns
T_{CCLK6}		6	Commercial	142	313	ns
			Industrial	121		ns
T_{CCLK12}		12	Commercial	71.2	157	ns
			Industrial	60.6		ns
T_{CCLK25}		25	Commercial	35.5	78.2	ns
			Industrial	30.3		ns
T_{CCLK50}		50	Commercial	17.8	39.1	ns
			Industrial	15.1		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream. See **Bitstream Generator (BitGen) Options** in Module 2.

Table 110: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	0.8	1.8	MHz
			Industrial		2.1	MHz
F_{CCLK3}		3	Commercial	1.6	3.6	MHz
			Industrial		4.2	MHz
F_{CCLK6}		6	Commercial	3.2	7.1	MHz
			Industrial		8.3	MHz
F_{CCLK12}		12	Commercial	6.4	14.1	MHz
			Industrial		16.5	MHz
F_{CCLK25}		25	Commercial	12.8	28.1	MHz
			Industrial		33.0	MHz
F_{CCLK50}		50	Commercial	25.6	56.2	MHz
			Industrial		66.0	MHz

Table 111: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		***ConfigRate* Setting**						Units
			1	**3**	**6**	**12**	**25**	**50**	
T_{MCCL}, T_{MCCH}	Master mode CCLK minimum Low and High time	Commercial	276	138	69	34.5	17.1	8.5	ns
		Industrial	235	117	58	29.3	14.5	7.3	ns

Table 112: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing

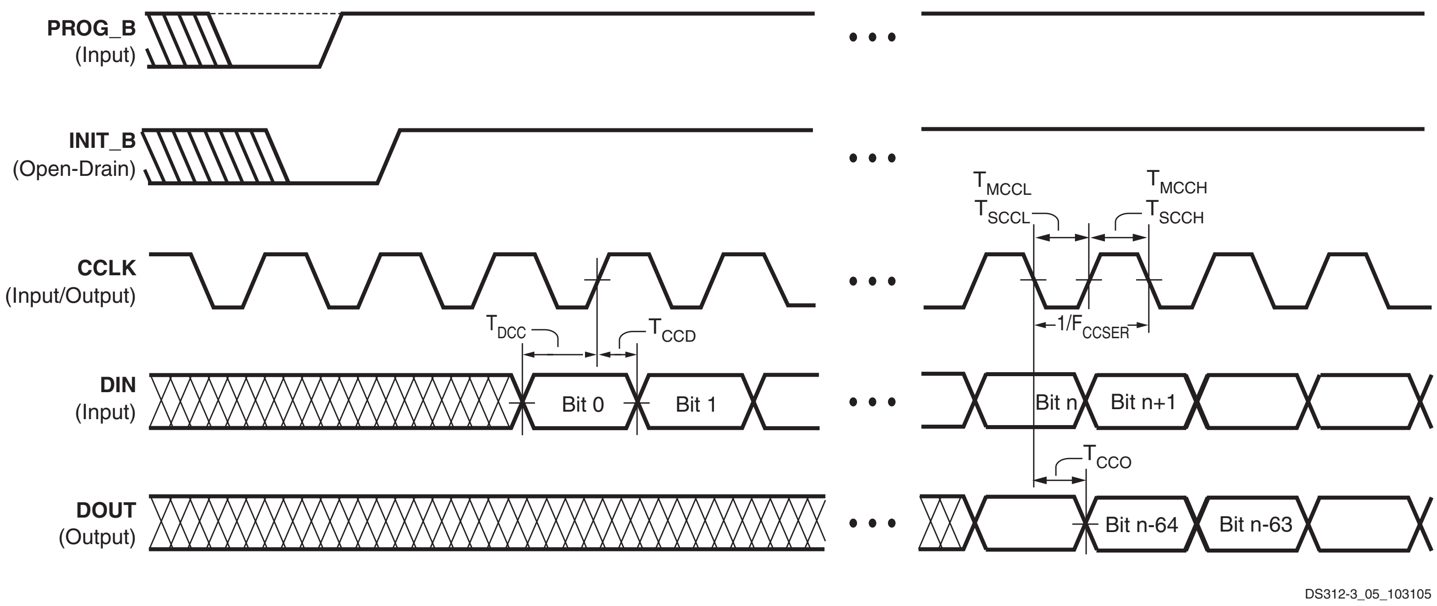


Figure 76: **Waveforms for Master Serial and Slave Serial Configuration**

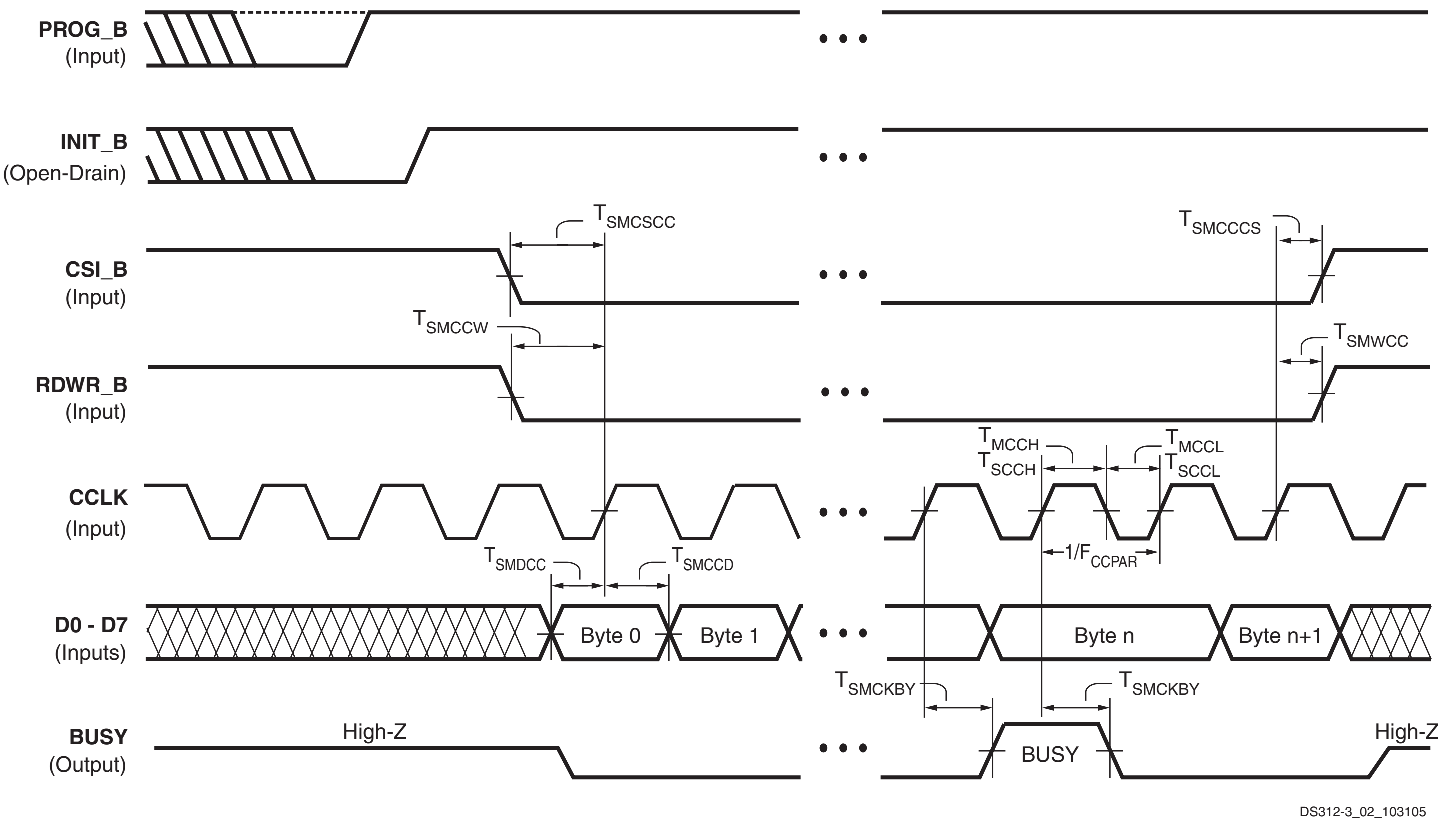
Table 113: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	11.0	-	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Both	0	-	ns
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 111		
			Slave	See Table 112		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 111		
			Slave	See Table 112		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Slave	0	66[2]	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 76.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CS_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CS_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0 - D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0 - D7 bus.

Figure 77: **Waveforms for Slave Parallel Configuration**

Table 114: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description	All Speed Grades		Units
		Min	Max	
Clock-to-Output Times				
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	-	12.0	ns
Setup Times				
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	11.0	-	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin	10.0	-	ns
T_{SMCCW}(2)	Setup time on the RDWR_B pin before the rising transition at the CCLK pin	23.0	-	ns

Table 114: **Timing for the Slave Parallel Configuration Mode *(Continued)***

Symbol	Description			All Speed Grades		Units
				Min	**Max**	
Hold Times						
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins			1.0	-	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin			0	-	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin			0	-	ns
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin			5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(2)	0	50	MHz
			Using the BUSY pin	0	66	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 76.
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
3. Some Xilinx documents refer to Parallel modes as "SelectMAP" modes.

Serial Peripheral Interface (SPI) Configuration Timing

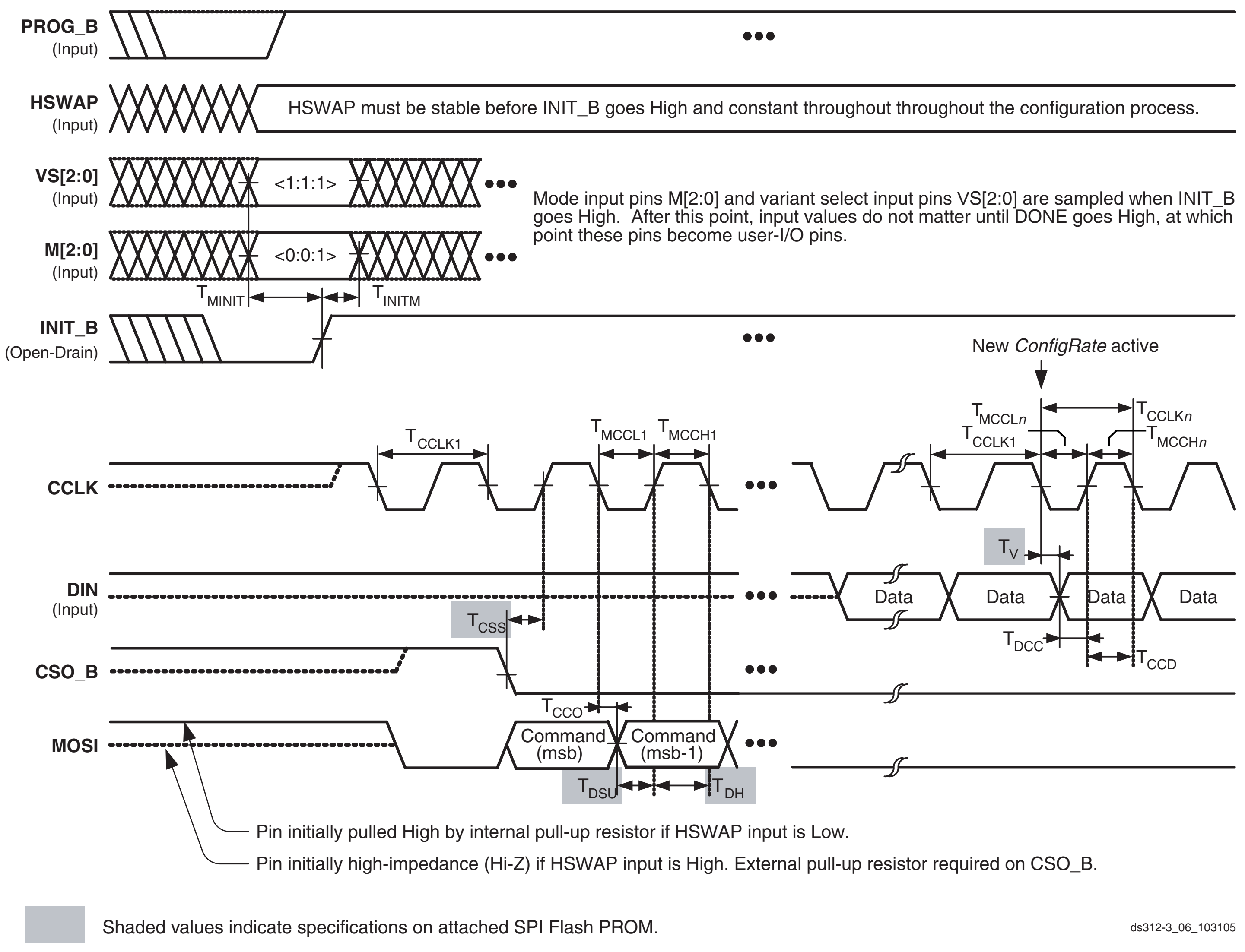


Figure 78: **Waveforms for Serial Peripheral Interface (SPI) Configuration**

Table 115: **Timing for Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	(see Table 109)		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	(see Table 109)		
T_{MINIT}	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B	50	-	ns
T_{INITM}	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B	0	-	ns
T_{CCO}	Address A[23:0] outputs valid after CCLK falling edge	See Table 113		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK falling edge	See Table 113		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK falling edge	See Table 113		

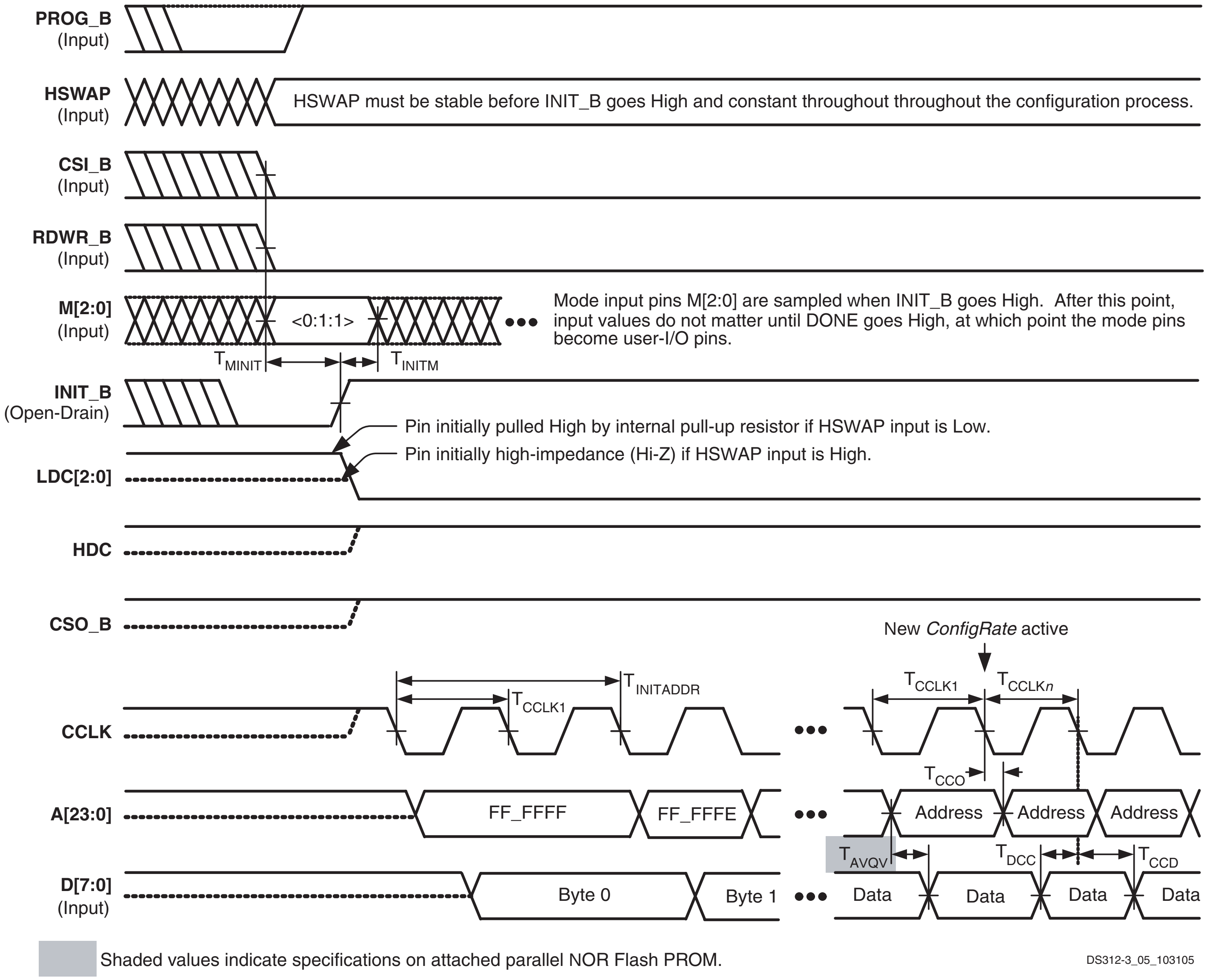
Table 116: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \le T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \le T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \le T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \le T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \ge \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA provides the CCLK frequency. The post-configuration requirements may be different, depending on the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.

Byte Peripheral Interface (BPI) Configuration Timing



▨ Shaded values indicate specifications on attached parallel NOR Flash PROM.

Figure 79: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration (BPI-DN mode shown)**

Table 117: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description		Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period		(see Table 109)		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting		(see Table 109)		
T_{MINIT}	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B		50	-	ns
T_{INITM}	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B		0	-	ns
$T_{INITADDR}$	Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid	**BPI-UP:** (M[2:0]=<0:1:0>)	5	5	T_{CCLK1} cycles
		BPI-DN: (M[2:0]=<0:1:1>)	2	2	

Table 117: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode *(Continued)***

Symbol	Description	Minimum	Maximum	Units
T_{CCO}	Address A[23:0] outputs valid after CCLK falling edge	See Table 113		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK falling edge	See Table 113		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK falling edge	See Table 113		

Table 118: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM chip-select time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post-configuration requirements might be different, depending on the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

Table 119: **MultiBoot Trigger (MBT) Timing**

Symbol	Description	Minimum	Maximum	Units
T_{MBT}	MultiBoot Trigger (MBT) Low pulse width required to initiate MultiBoot reconfiguration	300	∞	ns

Notes:

1. MutiBoot re-configuration starts on the rising edge after MBT is Low for at least the prescribed minimum period.

IEEE 1149.1/1553 JTAG Test Access Port Timing

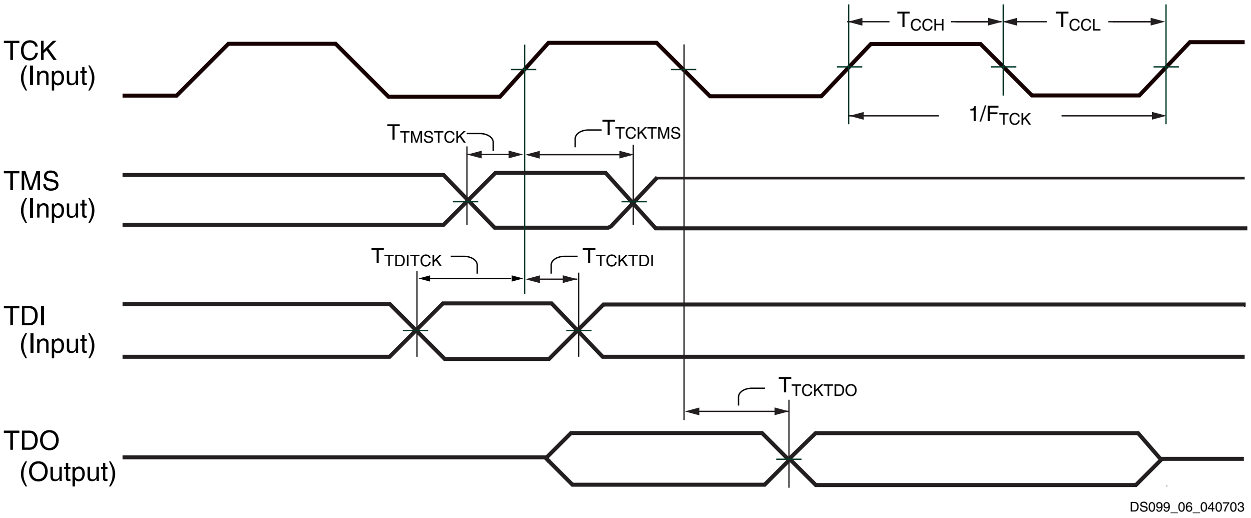


Figure 80: **JTAG Waveforms**

Table 120: **Timing for the JTAG Test Access Port**

Symbol	Description	All Speed Grades		Units
		Min	Max	
Clock-to-Output Times				
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns
Setup Times				
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	7.0	-	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	-	ns
Hold Times				
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	0	-	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	-	ns
Clock Timing				
T_{CCH}	The High pulse width at the TCK pin	5	-	ns
T_{CCL}	The Low pulse width at the TCK pin	5	-	ns
F_{TCK}	Frequency of the TCK signal	-	30	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 76.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
11/23/05	2.0	Added AC timing information and additional DC specifications.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Finalized production timing parameters. All speed grades for all Spartan-3E FPGAs are now Production status using the v1.21 speed files, as shown in Table 83. Expanded description in Note 2, Table 77. Updated pin-to-pin and clock-to-output timing based on final characterization, shown in Table 84. Updated system-synchronous input setup and hold times based on final characterization, shown in Table 85 and Table 86. Updated other I/O timing in Table 87. Provided input and output adjustments for LVPECL_25, DIFF_SSTL and DIFF_HSTL I/O standards that supersede the v1.21 speed file values, in Table 88 and Table 91. Reduced I/O three-state and set/reset delays in Table 90. Added XC3S100E FPGA in CP132 package to Table 93. Increased T_{AS} slice flip-flop timing by 100 ps in Table 95. Updated distributed RAM timing in Table 96 and SRL16 timing in Table 97. Updated global clock timing, removed left/right clock buffer limits in Table 98. Updated block RAM timing in Table 100. Added DCM parameters for remainder of Step 0 device; added improved Step 1 DCM peformance to Table 101, Table 102, Table 103, and Table 104. Added minimum INIT_B pulse width specification, T_{INIT}, in Table 108. Increased data hold time for Slave Parallel mode to 1.0 ns (T_{SMCCD}) in Table 114. Improved the DCM performance for the XC3S1200E, Stepping 0 in Table 101, Table 102, Table 103, and Table 104. Corrected links in Table 115 and Table 117. Added MultiBoot timing specifications to Table 119.
04/07/06	3.1	Improved SSO limits for LVDS_25, MINI_LVDS_25, and RSDS_25 I/O standards in the QFP packages (Table 94). Removed potentially confusing Note 2 from Table 77.
05/19/06	3.2	Clarified that 100 mV of hysteresis applies to LVCMOS33 and LVCMOS25 I/O standards (Note 4, Table 79). Other minor edits.

Spartan-3E FPGA Family: Pinout Descriptions

DS312-4 (v3.1) May 19, 2006

Preliminary Product Specification

Introduction

This section describes the various pins on a Spartan™-3E FPGA and how they connect within the supported component packages.

Pin Types

Most pins on a Spartan-3E FPGA are general-purpose, user-defined I/O pins. There are, however, up to 11 different functional types of pins on Spartan-3E packages, as outlined in Table 121. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 121: **Types of Pins on Spartan-3E FPGAs**

Type / Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure.	IP IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. Some of the dual-purpose pins are also shared with bottom-edge global (GCLK) or right-half (RHCLK) clock inputs . See the **Configuration** section in Module 2 for additional information on these signals.	M[2:0] HSWAP CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B BUSY/DOUT INIT_B A[23:20] A19/VS2 A18/VS1 A17/VS0 A[16:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxx_#/VREF_# IO/VREF_# IO_Lxx_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Every package has 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right-half of the device. The LHCLK inputs optionally clock the left-half of the device. Some of the clock pins are shared with the dual-purpose configuration pins and are considered DUAL-type. See the **Clocking Infrastructure** section in Module 2 for additional information on these signals.	IO_Lxx_#/GCLK[15:2], IP_Lxx_#/GCLK[1:0], IO_Lxx_#/LHCLK[7:0], IO_Lxx_#/RHCLK[7:0]

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All other trademarks are the property of their respective owners.

Table 121: **Types of Pins on Spartan-3E FPGAs *(Continued)***

Type / Color Code	Description	Pin Name(s) in Type
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the **Configuration** section in Module 2 for additional information on these signals.	DONE, PROG_B
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected to +2.5V. See the **Powering Spartan-3E FPGAs** section in Module 2 for additional information on this signal.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V. See the **Powering Spartan-3E FPGAs** section in Module 2 for additional information on this signal.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. See the **Powering Spartan-3E FPGAs** section in Module 2 for additional information on these signals.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.

I/Os with Lxxy_# are part of a differential output pair. 'L' indicates differential output capability. The "xx" field is a two-digit integer, unique to each bank that identifies a differential pin-pair. The 'y' field is either 'P' for the true signal or 'N' for the inverted signal in the differential pair. The '#' field is the I/O bank number.

Differential Pair Labeling

A pin supports differential standards if the pin is labeled in the format "Lxxy_#". The pin name suffix has the following significance. Figure 81 provides a specific example showing a differential input to and a differential output from Bank 1.

'L' indicates that the pin is part of a differentia**L** pair.

"xx" is a two-digit integer, unique for each bank, that identifies a differential pin-pair.

'y' is replaced by 'P' for the true signal or 'N' for the inverted. These two pins form one differential pin-pair.

'#' is an integer, 0 through 3, indicating the associated I/O bank.

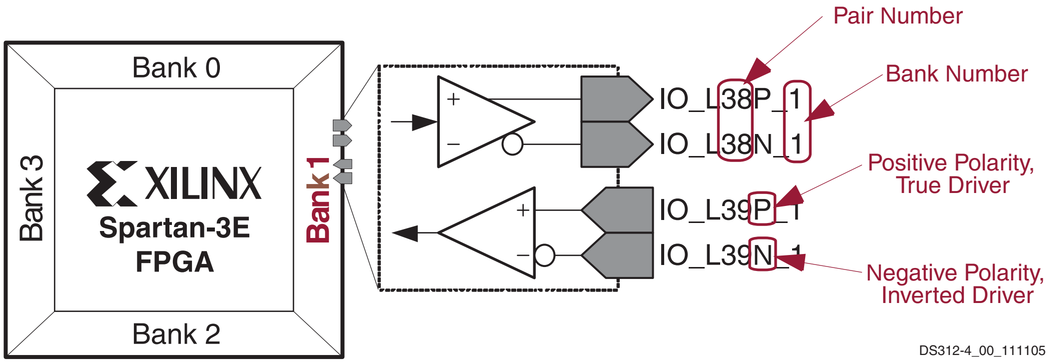


Figure 81: **Differential Pair Labeling**

Package Overview

Table 122 shows the eight low-cost, space-saving production package styles for the Spartan-3E family. Each package style is available as a standard and an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "VQ100" package becomes "VQG100" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 124.

Not all Spartan-3E densities are available in all packages. For a specific package, however, there is a common footprint that supports all the devices available in that package. See the footprint diagrams that follow.

For additional package information, see UG112: *Device Package User Guide*.

Table 122: **Spartan-3E Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass[1] (g)
VQ100 / VQG100	100	Very-thin Quad Flat Pack (VQFP)	66	0.5	16 x 16	1.20	0.6
CP132 / CPG132	132	Chip-Scale Package (CSP)	92	0.5	8.1 x 8.1	1.10	0.1
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	22 x 22	1.60	1.4
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	158	0.5	30.6 x 30.6	4.10	5.3
FT256 / FTG256	256	Fine-pitch, Thin Ball Grid Array (FBGA)	190	1.0	17 x 17	1.55	0.9
FG320 / FGG320	320	Fine-pitch Ball Grid Array (FBGA)	250	1.0	19 x 19	2.00	1.4
FG400 / FGG400	400	Fine-pitch Ball Grid Array (FBGA)	304	1.0	21 x 21	2.43	2.2
FG484 / FGG484	484	Fine-pitch Ball Grid Array (FBGA)	376	1.0	23 x 23	2.60	2.2

Notes:

1. Package mass is ±10%.

Selecting the Right Package Option

Spartan-3 FPGAs are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. While QFP packaging offers the lowest absolute cost, the BGA packages are superior in almost every other aspect, as summarized in Table 123. Consequently, Xilinx recommends using BGA packaging whenever possible.

Table 123: **QFP and BGA Comparison**

Characteristic	Quad Flat Pack (QFP)	Ball Grid Array (BGA)
Maximum User I/O	158	376
Packing Density (Logic/Area)	Good	Better
Signal Integrity	Fair	Better
Simultaneous Switching Output (SSO) Support	Fair	Better
Thermal Dissipation	Fair	Better
Minimum Printed Circuit Board (PCB) Layers	4	4-6
Hand Assembly/Rework	Possible	Difficult

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx website at the specified location in Table 124.

Table 124: **Xilinx Package Mechanical Drawings**

Package	Web Link (URL)
VQ100 / VQG100	http://www.xilinx.com/bvdocs/packages/vq100.pdf
CP132 / CPG132	http://www.xilinx.com/bvdocs/packages/cp132.pdf
TQ144 / TQG144	http://www.xilinx.com/bvdocs/packages/tq144.pdf
PQ208 / PQG208	http://www.xilinx.com/bvdocs/packages/pq208.pdf
FT256 / FTG256	http://www.xilinx.com/bvdocs/packages/ft256.pdf
FG320 / FGG320	http://www.xilinx.com/bvdocs/packages/fg320.pdf
FG400 / FGG400	http://www.xilinx.com/bvdocs/packages/fg400.pdf
FG484 / FGG484	http://www.xilinx.com/bvdocs/packages/fg484.pdf

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 125.

Table 125: **Power and Ground Supply Pins by Package**

Package	VCCINT	VCCAUX	VCCO	GND
VQ100	4	4	8	12
CP132	6	4	8	16
TQ144	4	4	9	13
PQ208	4	8	12	20
FT256	8	8	16	28
FG320	8	8	20	28
FG400	16	8	24	42
FG484	16	10	28	48

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/O depend on the device type and the package in which it is available, as shown in Table 126. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—i.e., N.C.—pins on the device.

Table 126: **Maximum User I/O by Package**

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF	CLK[1]	N.C.
XC3S100E	VQ100	66	7	30	16	1	21	4	24	0
XC3S250E		66	7	30	16	1	21	4	24	0
XC3S100E	CP132	83	11	35	16	2	42	7	16	9
XC3S250E		92	7	41	22	0	46	8	16	0
XC3S500E		92	7	41	22	0	46	8	16	0
XC3S100E	TQ144	108	28	40	22	19	42	9	16	0
XC3S250E		108	28	40	20	21	42	9	16	0
XC3S250E	PQ208	158	32	65	58	25	46	13	16	0
XC3S500E		158	32	65	58	25	46	13	16	0
XC3S250E	FT256	172	40	68	62	33	46	15	16	16
XC3S500E		190	41	77	76	33	46	19	16	0
XC3S1200E		190	40	77	78	31	46	19	16	0
XC3S500E	FG320	232	56	92	102	48	46	20	16	18
XC3S1200E		250	56	99	120	47	46	21	16	0
XC3S1600E		250	56	99	120	47	46	21	16	0
XC3S1200E	FG400	304	72	124	156	62	46	24	16	0
XC3S1600E		304	72	124	156	62	46	24	16	0
XC3S1600E	FG484	376	82	156	214	72	46	28	16	0

Notes:

1. All devices have 24 possible global clock and right- and left-half side clock inputs. The right-half and bottom-edge clock pins have shared functionality in some FPGA configuration modes. Consequently, some clocks pins are counted in the DUAL column.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Download the files from the following location: Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

http://www.xilinx.com/bvdocs/publications/s3e_pin.zip

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3E FPGA is reported using either the Web Power Tool estimator or the XPower calculator integrated in the Xilinx ISE development software. Table 127 provides the thermal characteristics for the various Spartan-3E package offerings.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference per watt between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The “Still Air (0 LFM)” column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 127: **Spartan-3E Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows: Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	Units
VQ100	XC3S100E	13.0	30.9	49.0	40.7	37.9	37.0	°C/Watt
	XC3S250E	11.0	25.9	43.3	36.0	33.6	32.7	°C/Watt
CP132	XC3S100E	TBD	TBD	TBD	TBD	TBD	TBD	°C/Watt
	XC3S250E	11.8	28.4	48.5	42.0	39.6	38.1	°C/Watt
	XC3S500E	8.5	21.1	41.4	35.0	32.8	31.4	°C/Watt
TQ144	XC3S100E	8.2	31.9	52.1	40.5	34.6	32.5	°C/Watt
	XC3S250E	7.2	25.7	37.6	29.2	25.0	23.4	°C/Watt
PQ208	XC3S250E	9.8	29.0	37.0	27.3	24.1	22.4	°C/Watt
	XC3S500E	8.5	26.8	36.1	26.6	23.6	21.8	°C/Watt
FT256	XC3S250E	12.4	27.6	35.8	29.4	28.4	28.1	°C/Watt
	XC3S500E	9.7	22.3	31.1	25.0	24.0	23.6	°C/Watt
	XC3S1200E	6.5	16.4	26.3	20.6	19.4	19.0	°C/Watt
FG320	XC3S500E	13.0	17.1	25.9	20.4	19.2	18.5	°C/Watt
	XC3S1200E	10.2	13.8	22.7	17.4	16.1	15.4	°C/Watt
	XC3S1600E	8.8	12.1	20.8	15.3	14.0	13.3	°C/Watt
FG400	XC3S1200E	9.7	13.5	22.2	17.1	15.9	15.2	°C/Watt
	XC3S1600E	8.3	11.6	20.1	15.1	13.9	13.2	°C/Watt
FG484	XC3S1600E	7.8	11.3	16.7	12.2	11.0	10.5	°C/Watt

VQ100: 100-lead Very-thin Quad Flat Package

The XC3S100E and the XC3S250E devices are available in the 100-lead very-thin quad flat package, VQ100. Both devices share a common footprint for this package as shown in Table 128 and Figure 82.

Table 128 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The VQ100 package does not support the Byte-wide Peripheral Interface (BPI) configuration mode. Consequently, the VQ100 footprint has fewer DUAL-type pins than other packages.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at http://www.xilinx.com/bvdocs/publications/s3e_pin.zip.

Pinout Table

Table 128 shows the pinout for production Spartan-3E FPGAs in the VQ100 package.

Table 128: **VQ100 Package Pinout**

Bank	XC3S100E XC3S250E Pin Name	VQ100 Pin Number	Type
0	IO	P92	I/O
0	IO_L01N_0	P79	I/O
0	IO_L01P_0	P78	I/O
0	IO_L02N_0/GCLK5	P84	GCLK
0	IO_L02P_0/GCLK4	P83	GCLK
0	IO_L03N_0/GCLK7	P86	GCLK
0	IO_L03P_0/GCLK6	P85	GCLK
0	IO_L05N_0/GCLK11	P91	GCLK
0	IO_L05P_0/GCLK10	P90	GCLK
0	IO_L06N_0/VREF_0	P95	VREF
0	IO_L06P_0	P94	I/O
0	IO_L07N_0/HSWAP	P99	DUAL
0	IO_L07P_0	P98	I/O
0	IP_L04N_0/GCLK9	P89	GCLK
0	IP_L04P_0/GCLK8	P88	GCLK
0	VCCO_0	P82	VCCO
0	VCCO_0	P97	VCCO
1	IO_L01N_1	P54	I/O
1	IO_L01P_1	P53	I/O
1	IO_L02N_1	P58	I/O
1	IO_L02P_1	P57	I/O
1	IO_L03N_1/RHCLK1	P61	RHCLK
1	IO_L03P_1/RHCLK0	P60	RHCLK
1	IO_L04N_1/RHCLK3	P63	RHCLK
1	IO_L04P_1/RHCLK2	P62	RHCLK
1	IO_L05N_1/RHCLK5	P66	RHCLK
1	IO_L05P_1/RHCLK4	P65	RHCLK
1	IO_L06N_1/RHCLK7	P68	RHCLK
1	IO_L06P_1/RHCLK6	P67	RHCLK
1	IO_L07N_1	P71	I/O
1	IO_L07P_1	P70	I/O
1	IP/VREF_1	P69	VREF
1	VCCO_1	P55	VCCO
1	VCCO_1	P73	VCCO
2	IO/D5	P34	DUAL
2	IO/M1	P42	DUAL
2	IO_L01N_2/INIT_B	P25	DUAL
2	IO_L01P_2/CSO_B	P24	DUAL
2	IO_L02N_2/MOSI/CSI_B	P27	DUAL
2	IO_L02P_2/DOUT/BUSY	P26	DUAL
2	IO_L03N_2/D6/GCLK13	P33	DUAL/GCLK
2	IO_L03P_2/D7/GCLK12	P32	DUAL/GCLK
2	IO_L04N_2/D3/GCLK15	P36	DUAL/GCLK
2	IO_L04P_2/D4/GCLK14	P35	DUAL/GCLK
2	IO_L06N_2/D1/GCLK3	P41	DUAL/GCLK
2	IO_L06P_2/D2/GCLK2	P40	DUAL/GCLK
2	IO_L07N_2/DIN/D0	P44	DUAL
2	IO_L07P_2/M0	P43	DUAL
2	IO_L08N_2/VS1	P48	DUAL
2	IO_L08P_2/VS2	P47	DUAL
2	IO_L09N_2/CCLK	P50	DUAL
2	IO_L09P_2/VS0	P49	DUAL
2	IP/VREF_2	P30	VREF
2	IP_L05N_2/M2/GCLK1	P39	DUAL/GCLK
2	IP_L05P_2/RDWR_B/ GCLK0	P38	DUAL/GCLK
2	VCCO_2	P31	VCCO
2	VCCO_2	P45	VCCO
3	IO_L01N_3	P3	I/O
3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	P5	VREF

Table 128: **VQ100 Package Pinout *(Continued)***

Bank	XC3S100E XC3S250E Pin Name	VQ100 Pin Number	Type
3	IO_L02P_3	P4	I/O
3	IO_L03N_3/LHCLK1	P10	LHCLK
3	IO_L03P_3/LHCLK0	P9	LHCLK
3	IO_L04N_3/LHCLK3	P12	LHCLK
3	IO_L04P_3/LHCLK2	P11	LHCLK
3	IO_L05N_3/LHCLK5	P16	LHCLK
3	IO_L05P_3/LHCLK4	P15	LHCLK
3	IO_L06N_3/LHCLK7	P18	LHCLK
3	IO_L06P_3/LHCLK6	P17	LHCLK
3	IO_L07N_3	P23	I/O
3	IO_L07P_3	P22	I/O
3	IP	P13	INPUT
3	VCCO_3	P8	VCCO
3	VCCO_3	P20	VCCO
GND	GND	P7	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P29	GND
GND	GND	P37	GND
GND	GND	P52	GND
GND	GND	P59	GND
GND	GND	P64	GND
GND	GND	P72	GND
GND	GND	P81	GND
GND	GND	P87	GND
GND	GND	P93	GND
VCCAUX	DONE	P51	CONFIG
VCCAUX	PROG_B	P1	CONFIG
VCCAUX	TCK	P77	JTAG
VCCAUX	TDI	P100	JTAG
VCCAUX	TDO	P76	JTAG
VCCAUX	TMS	P75	JTAG
VCCAUX	VCCAUX	P21	VCCAUX
VCCAUX	VCCAUX	P46	VCCAUX
VCCAUX	VCCAUX	P74	VCCAUX
VCCAUX	VCCAUX	P96	VCCAUX
VCCINT	VCCINT	P6	VCCINT
VCCINT	VCCINT	P28	VCCINT
VCCINT	VCCINT	P56	VCCINT
VCCINT	VCCINT	P80	VCCINT

User I/Os by Bank

Table 129 indicates how the 66 available user-I/O pins are distributed between the four I/O banks on the VQ100 package.

Table 129: **User I/Os Per Bank for XC3S100E and XC3S250E in the VQ100 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	15	5	0	1	1	8
Right	1	15	6	0	0	1	8
Bottom	2	19	0	0	18	1	0(1)
Left	3	17	5	1	2	1	8
TOTAL		**66**	**16**	**1**	**21**	**4**	**24**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

The production XC3S100E and XC3S250E FPGAs have identical footprints in the VQ100 package. Designs can migrate between the XC3S100E and XC3S250E without further consideration.

VQ100 Footprint

In Figure 82, note pin 1 indicator in top-left corner and logo orientation.

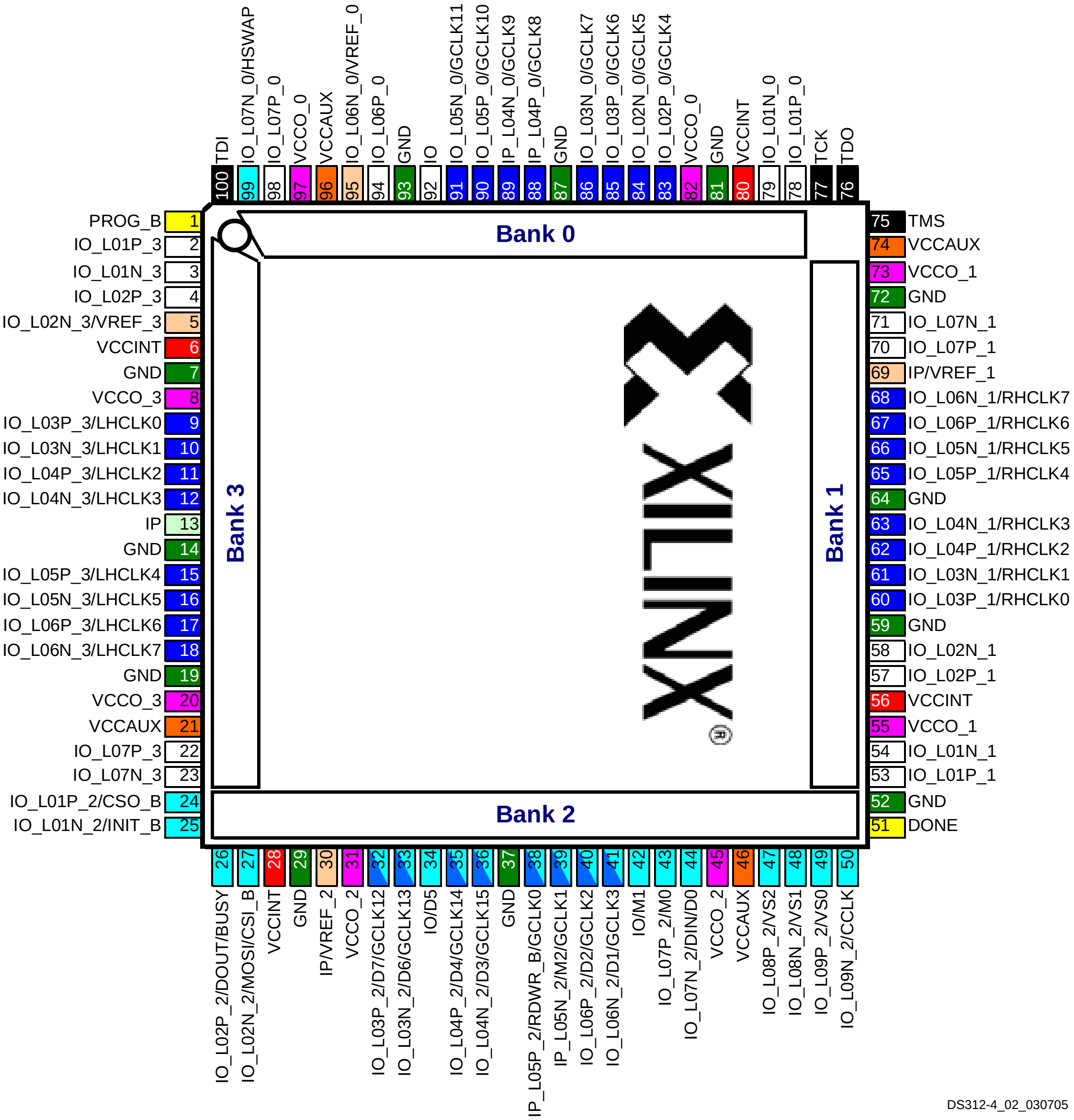


Figure 82: **VQ100 Package Footprint (top view).**

16	**I/O:** Unrestricted, general-purpose user I/O	21	**DUAL:** Configuration pin, then possible user-I/O	4	**VREF:** User I/O or input voltage reference for bank
1	**INPUT:** Unrestricted, general-purpose input pin	24	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	12	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

CP132: 132-ball Chip-scale Package

The XC3S100E, XC3S250E and the XC3S500E FPGAs are available in the 132-ball chip-scale package, CP132. The devices share a common footprint for this package as shown in Table 130 and Figure 83.

Table 130 lists all the CP132 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

Physically, the D14 and K2 balls on the XC3S100E and XC3S250E FPGAs are not connected but should be connected to VCCINT to maintain density migration compatibility.

Similarly, the A4, C1, and P10 balls on the XC3S100E FPGA are not connected but should be connected to GND to maintain density migration compatibility.

The XC3S100E FPGA has four fewer BPI address pins, A[19:0], whereas the XC3S250E and XC3S500E support A[23:0].

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3e_pin.zip.

Pinout Table

Table 130: **CP132 Package Pinout**

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
0	IO_L01N_0	IO_L01N_0	C12	I/O
0	IO_L01P_0	IO_L01P_0	A13	I/O
0	N.C. (◆)	IO_L02N_0	A12	***100E:*** N.C. ***Others:*** I/O
0	N.C. (◆)	IO_L02P_0	B12	***100E:*** N.C. ***Others:*** I/O
0	N.C. (◆)	IO_L03N_0/VREF_0	B11	***100E:*** N.C. ***Others:*** VREF (I/O)
0	IP	IO_L03P_0	C11	***100E:*** INPUT ***Others:*** I/O
0	IO_L04N_0/GCLK5	IO_L04N_0/GCLK5	C9	GCLK
0	IO_L04P_0/GCLK4	IO_L04P_0/GCLK4	A10	GCLK
0	IO_L05N_0/GCLK7	IO_L05N_0/GCLK7	A9	GCLK
0	IO_L05P_0/GCLK6	IO_L05P_0/GCLK6	B9	GCLK
0	IO_L07N_0/GCLK11	IO_L07N_0/GCLK11	B7	GCLK
0	IO_L07P_0/GCLK10	IO_L07P_0/GCLK10	A7	GCLK
0	IO_L08N_0/VREF_0	IO_L08N_0/VREF_0	C6	VREF
0	IO_L08P_0	IO_L08P_0	B6	I/O
0	IO_L09N_0	IO_L09N_0	C5	I/O
0	IO_L09P_0	IO_L09P_0	B5	I/O
0	N.C. (◆)	IO_L10N_0	C4	***100E:*** N.C. ***Others:*** I/O
0	IP	IO_L10P_0	B4	***100E:*** INPUT ***Others:*** I/O
0	IO_L11N_0/HSWAP	IO_L11N_0/HSWAP	B3	DUAL
0	IO_L11P_0	IO_L11P_0	A3	I/O
0	IP_L06N_0/GCLK9	IP_L06N_0/GCLK9	C8	GCLK
0	IP_L06P_0/GCLK8	IP_L06P_0/GCLK8	B8	GCLK

Table 130: **CP132 Package Pinout *(Continued)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
0	VCCO_0	VCCO_0	A6	VCCO
0	VCCO_0	VCCO_0	B10	VCCO
1	IO/A0	IO/A0	F12	DUAL
1	IO/VREF_1	IO/VREF_1	K13	VREF
1	IO_L01N_1/A15	IO_L01N_1/A15	N14	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	N13	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	M13	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	M12	DUAL
1	IO_L03N_1/A11	IO_L03N_1/A11	L14	DUAL
1	IO_L03P_1/A12	IO_L03P_1/A12	L13	DUAL
1	IO_L04N_1/A9/RHCLK1	IO_L04N_1/A9/RHCLK1	J12	RHCLK/DUAL
1	IO_L04P_1/A10/RHCLK0	IO_L04P_1/A10/RHCLK0	K14	RHCLK/DUAL
1	IO_L05N_1/A7/RHCLK3/TRDY1	IO_L05N_1/A7/RHCLK3/TRDY1	J14	RHCLK/DUAL
1	IO_L05P_1/A8/RHCLK2	IO_L05P_1/A8/RHCLK2	J13	RHCLK/DUAL
1	IO_L06N_1/A5/RHCLK5	IO_L06N_1/A5/RHCLK5	H12	RHCLK/DUAL
1	IO_L06P_1/A6/RHCLK4/IRDY1	IO_L06P_1/A6/RHCLK4/IRDY1	H13	RHCLK/DUAL
1	IO_L07N_1/A3/RHCLK7	IO_L07N_1/A3/RHCLK7	G13	RHCLK/DUAL
1	IO_L07P_1/A4/RHCLK6	IO_L07P_1/A4/RHCLK6	G14	RHCLK/DUAL
1	IO_L08N_1/A1	IO_L08N_1/A1	F13	DUAL
1	IO_L08P_1/A2	IO_L08P_1/A2	F14	DUAL
1	IO_L09N_1/LDC0	IO_L09N_1/LDC0	D12	DUAL
1	IO_L09P_1/HDC	IO_L09P_1/HDC	D13	DUAL
1	IO_L10N_1/LDC2	IO_L10N_1/LDC2	C13	DUAL
1	IO_L10P_1/LDC1	IO_L10P_1/LDC1	C14	DUAL
1	IP/VREF_1	IP/VREF_1	G12	VREF
1	VCCO_1	VCCO_1	E13	VCCO
1	VCCO_1	VCCO_1	M14	VCCO
2	IO/D5	IO/D5	P4	DUAL
2	IO/M1	IO/M1	N7	DUAL
2	IP/VREF_2	IO/VREF_2	P11	***100E:*** VREF(INPUT) ***Others:*** VREF(I/O)
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	N1	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	M2	DUAL
2	IO_L02N_2/MOSI/CSI_B	IO_L02N_2/MOSI/CSI_B	N2	DUAL
2	IO_L02P_2/DOUT/BUSY	IO_L02P_2/DOUT/BUSY	P1	DUAL
2	IO_L03N_2/D6/GCLK13	IO_L03N_2/D6/GCLK13	N4	DUAL/GCLK
2	IO_L03P_2/D7/GCLK12	IO_L03P_2/D7/GCLK12	M4	DUAL/GCLK
2	IO_L04N_2/D3/GCLK15	IO_L04N_2/D3/GCLK15	N5	DUAL/GCLK
2	IO_L04P_2/D4/GCLK14	IO_L04P_2/D4/GCLK14	M5	DUAL/GCLK
2	IO_L06N_2/D1/GCLK3	IO_L06N_2/D1/GCLK3	P7	DUAL/GCLK

Table 130: **CP132 Package Pinout *(Continued)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
2	IO_L06P_2/D2/GCLK2	IO_L06P_2/D2/GCLK2	P6	DUAL/GCLK
2	IO_L07N_2/DIN/D0	IO_L07N_2/DIN/D0	N8	DUAL
2	IO_L07P_2/M0	IO_L07P_2/M0	P8	DUAL
2	N.C. (◆)	IO_L08N_2/A22	M9	***100E:*** N.C. ***Others:*** DUAL
2	N.C. (◆)	IO_L08P_2/A23	N9	***100E:*** N.C. ***Others:*** DUAL
2	N.C. (◆)	IO_L09N_2/A20	M10	***100E:*** N.C. ***Others:*** DUAL
2	N.C. (◆)	IO_L09P_2/A21	N10	***100E:*** N.C. ***Others:*** DUAL
2	IO_L10N_2/VS1/A18	IO_L10N_2/VS1/A18	M11	DUAL
2	IO_L10P_2/VS2/A19	IO_L10P_2/VS2/A19	N11	DUAL
2	IO_L11N_2/CCLK	IO_L11N_2/CCLK	N12	DUAL
2	IO_L11P_2/VS0/A17	IO_L11P_2/VS0/A17	P12	DUAL
2	IP/VREF_2	IP/VREF_2	N3	VREF
2	IP_L05N_2/M2/GCLK1	IP_L05N_2/M2/GCLK1	N6	DUAL/GCLK
2	IP_L05P_2/RDWR_B/GCLK0	IP_L05P_2/RDWR_B/GCLK0	M6	DUAL/GCLK
2	VCCO_2	VCCO_2	M8	VCCO
2	VCCO_2	VCCO_2	P3	VCCO
3	IO	IO	J3	I/O
3	IP/VREF_3	IO/VREF_3	K3	***100E:*** VREF(INPUT) ***Others:*** VREF(I/O)
3	IO_L01N_3	IO_L01N_3	B1	I/O
3	IO_L01P_3	IO_L01P_3	B2	I/O
3	IO_L02N_3	IO_L02N_3	C2	I/O
3	IO_L02P_3	IO_L02P_3	C3	I/O
3	N.C. (◆)	IO_L03N_3	D1	***100E:*** N.C. ***Others:*** I/O
3	IO	IO_L03P_3	D2	I/O
3	IO_L04N_3/LHCLK1	IO_L04N_3/LHCLK1	F2	LHCLK
3	IO_L04P_3/LHCLK0	IO_L04P_3/LHCLK0	F3	LHCLK
3	IO_L05N_3/LHCLK3/IRDY2	IO_L05N_3/LHCLK3/IRDY2	G1	LHCLK
3	IO_L05P_3/LHCLK2	IO_L05P_3/LHCLK2	F1	LHCLK
3	IO_L06N_3/LHCLK5	IO_L06N_3/LHCLK5	H1	LHCLK
3	IO_L06P_3/LHCLK4/TRDY2	IO_L06P_3/LHCLK4/TRDY2	G3	LHCLK
3	IO_L07N_3/LHCLK7	IO_L07N_3/LHCLK7	H3	LHCLK
3	IO_L07P_3/LHCLK6	IO_L07P_3/LHCLK6	H2	LHCLK
3	IO_L08N_3	IO_L08N_3	L2	I/O
3	IO_L08P_3	IO_L08P_3	L1	I/O
3	IO_L09N_3	IO_L09N_3	M1	I/O

Table 130: **CP132 Package Pinout *(Continued)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
3	IO_L09P_3	IO_L09P_3	L3	I/O
3	IP/VREF_3	IP/VREF_3	E2	VREF
3	VCCO_3	VCCO_3	E1	VCCO
3	VCCO_3	VCCO_3	J2	VCCO
GND	N.C. (GND)	GND	A4	GND
GND	GND	GND	A8	GND
GND	N.C. (GND)	GND	C1	GND
GND	GND	GND	C7	GND
GND	GND	GND	C10	GND
GND	GND	GND	E3	GND
GND	GND	GND	E14	GND
GND	GND	GND	G2	GND
GND	GND	GND	H14	GND
GND	GND	GND	J1	GND
GND	GND	GND	K12	GND
GND	GND	GND	M3	GND
GND	GND	GND	M7	GND
GND	GND	GND	P5	GND
GND	N.C. (GND)	GND	P10	GND
GND	GND	GND	P14	GND
VCCAUX	DONE	DONE	P13	CONFIG
VCCAUX	PROG_B	PROG_B	A1	CONFIG
VCCAUX	TCK	TCK	B13	JTAG
VCCAUX	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	A14	JTAG
VCCAUX	TMS	TMS	B14	JTAG
VCCAUX	VCCAUX	VCCAUX	A5	VCCAUX
VCCAUX	VCCAUX	VCCAUX	E12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	K1	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P9	VCCAUX
VCCINT	VCCINT	VCCINT	A11	VCCINT
VCCINT	VCCINT	VCCINT	D3	VCCINT
VCCINT	N.C. (VCCINT)	VCCINT	D14	VCCINT
VCCINT	N.C. (VCCINT)	VCCINT	K2	VCCINT
VCCINT	VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	VCCINT	P2	VCCINT

User I/Os by Bank

Table 131 shows how the 83 available user-I/O pins are distributed on the XC3S100E FPGA packaged in the CP132 package. Table 132 indicates how the 92 available user-I/O pins are distributed on the XC3S250E and the XC3S500E FPGAs in the CP132 package.

Table 131: **User I/Os Per Bank for the XC3S100E in the CP132 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	18	6	2	1	1	8
Right	1	23	0	0	21	2	0(1)
Bottom	2	22	0	0	20	2	0(1)
Left	3	20	10	0	0	2	8
TOTAL		**83**	**16**	**2**	**42**	**7**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 132: **User I/Os Per Bank for the XC3S250E and XC3S500E in the CP132 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	22	11	0	1	2	8
Right	1	23	0	0	21	2	0(1)
Bottom	2	26	0	0	24	2	0(1)
Left	3	21	11	0	0	2	8
TOTAL		**92**	**22**	**0**	**46**	**8**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

Table 133 summarizes any footprint and functionality differences between the XC3S100E, the XC3S250E, and the XC3S500E FPGAs that may affect easy migration between devices in the CP132 package. There are 14 such balls. All other pins not listed in Table 133 unconditionally migrate between Spartan-3E devices available in the CP132 package.

The XC3S100E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S250E and the XC3S500E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

The XC3S100E FPGA in the CP132 package has four fewer BPI-mode address lines than the XC3S250E and XC3S500E.

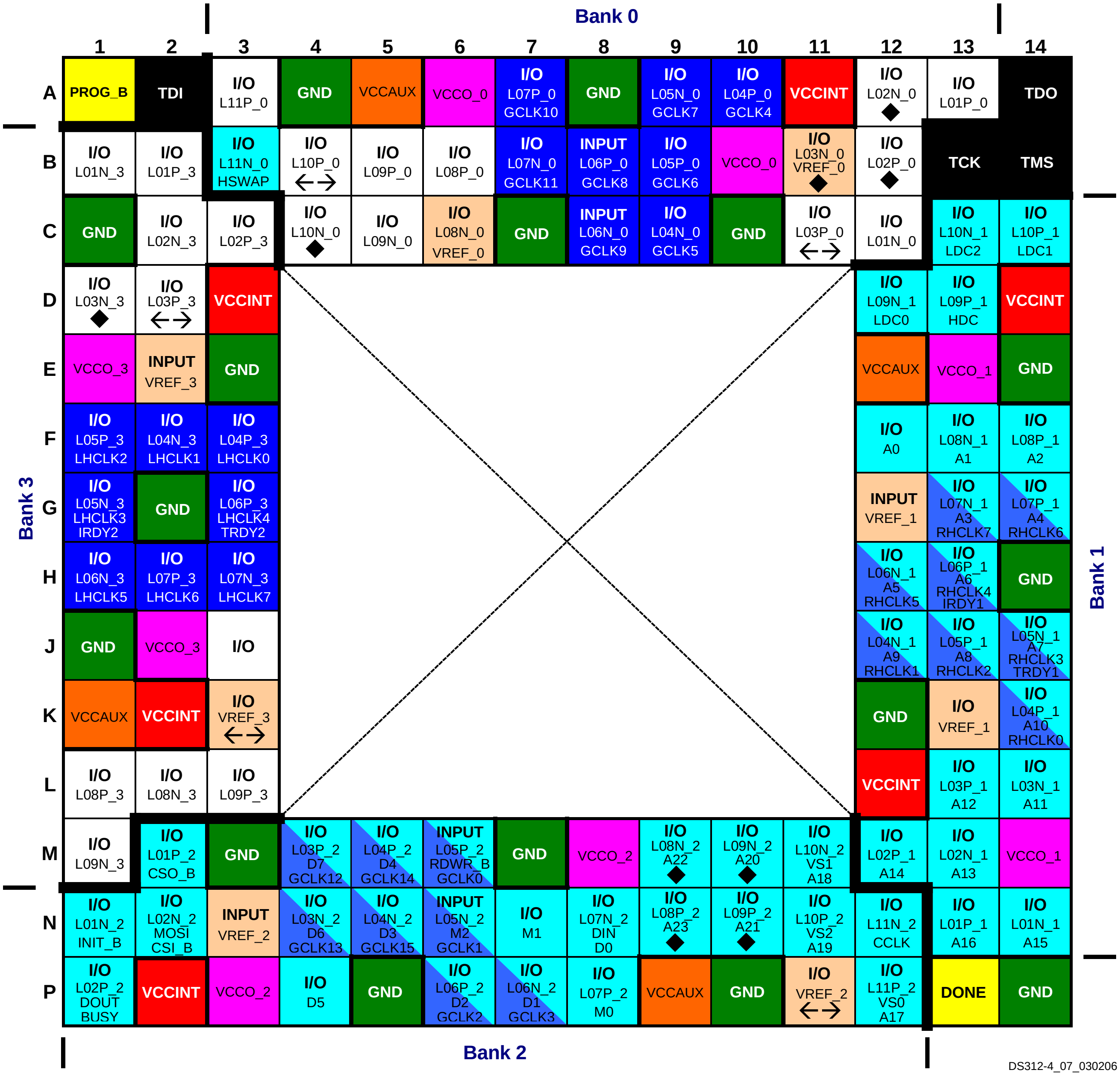
Table 133: **CP132 Footprint Migration Differences**

CP132 Ball	Bank	XC3S100E Type	Migration	XC3S250E Type	Migration	XC3S500E Type	Migration	XC3S100E Type
A12	0	N.C.	→	I/O	←→	I/O	←	N.C.
B4	0	INPUT	→	I/O	←→	I/O	←	INPUT
B11	0	N.C.	→	I/O	←→	I/O	←	N.C.
B12	0	N.C.	→	I/O	←→	I/O	←	N.C.
C4	0	N.C.	→	I/O	←→	I/O	←	N.C.
C11	0	INPUT	→	I/O	←→	I/O	←	INPUT
D1	3	N.C.	→	I/O	←→	I/O	←	N.C.
D2	3	I/O	→	I/O (Diff)	←→	I/O (Diff)	←	I/O
K3	3	VREF(INPUT)	→	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)
M9	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
M10	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
N9	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
N10	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
P11	2	VREF(INPUT)	→	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)
DIFFERENCES			**14**		**0**		**14**	

Legend:

←→	This pin is identical on the device on the left and the right.
→	This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.
←	This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

CP132 Footprint



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PROG_B	TDI	I/O L11P_0	GND	VCCAUX	VCCO_0	I/O L07P_0 GCLK10	GND	I/O L05N_0 GCLK7	I/O L04P_0 GCLK4	VCCINT	I/O L02N_0 ◆	I/O L01P_0	TDO
B	I/O L01N_3	I/O L01P_3	I/O L11N_0 HSWAP	I/O L10P_0 ←→	I/O L09P_0	I/O L08P_0	I/O L07N_0 GCLK11	INPUT L06P_0 GCLK8	I/O L05P_0 GCLK6	VCCO_0	I/O L03N_0 VREF_0 ◆	I/O L02P_0 ◆	TCK	TMS
C	GND	I/O L02N_3	I/O L02P_3	I/O L10N_0 ◆	I/O L09N_0	I/O L08N_0 VREF_0	GND	INPUT L06N_0 GCLK9	I/O L04N_0 GCLK5	GND	I/O L03P_0 ←→	I/O L01N_0	I/O L10N_1 LDC2	I/O L10P_1 LDC1
D	I/O L03N_3 ◆	I/O L03P_3 ←→	VCCINT									I/O L09N_1 LDC0	I/O L09P_1 HDC	VCCINT
E	VCCO_3	INPUT VREF_3	GND									VCCAUX	VCCO_1	GND
F	I/O L05P_3 LHCLK2	I/O L04N_3 LHCLK1	I/O L04P_3 LHCLK0									I/O A0	I/O L08N_1 A1	I/O L08P_1 A2
G	I/O L05N_3 LHCLK3 IRDY2	GND	I/O L06P_3 LHCLK4 TRDY2									INPUT VREF_1	I/O L07N_1 A3 RHCLK7	I/O L07P_1 A4 RHCLK6
H	I/O L06N_3 LHCLK5	I/O L07P_3 LHCLK6	I/O L07N_3 LHCLK7									I/O L06N_1 A5 RHCLK5	I/O L06P_1 A6 RHCLK4 IRDY1	GND
J	GND	VCCO_3	I/O									I/O L04N_1 A9 RHCLK1	I/O L05P_1 A8 RHCLK2	I/O L05N_1 A7 RHCLK3 TRDY1
K	VCCAUX	VCCINT	I/O VREF_3 ←→									GND	I/O VREF_1	I/O L04P_1 A10 RHCLK0
L	I/O L08P_3	I/O L08N_3	I/O L09P_3									VCCINT	I/O L03P_1 A12	I/O L03N_1 A11
M	I/O L09N_3	I/O L01P_2 CSO_B	GND	I/O L03P_2 D7 GCLK12	I/O L04P_2 D4 GCLK14	INPUT L05P_2 RDWR_B GCLK0	GND	VCCO_2	I/O L08N_2 A22 ◆	I/O L09N_2 A20 ◆	I/O L10N_2 VS1 A18	I/O L02P_1 A14	I/O L02N_1 A13	VCCO_1
N	I/O L01N_2 INIT_B	I/O L02N_2 MOSI CSI_B	INPUT VREF_2	I/O L03N_2 D6 GCLK13	I/O L04N_2 D3 GCLK15	INPUT L05N_2 M2 GCLK1	I/O M1	I/O L07N_2 DIN D0	I/O L08P_2 A23 ◆	I/O L09P_2 A21 ◆	I/O L10P_2 VS2 A19	I/O L11N_2 CCLK	I/O L01P_1 A16	I/O L01N_1 A15
P	I/O L02P_2 DOUT BUSY	VCCINT	VCCO_2	I/O D5	GND	I/O L06P_2 D2 GCLK2	I/O L06N_2 D1 GCLK3	I/O L07P_2 M0	VCCAUX	GND	I/O VREF_2 ←→	I/O L11P_2 VS0 A17	DONE	GND

Figure 83: **CP132 Package Footprint (top view)**

16 to 22	**I/O:** Unrestricted, general-purpose user I/O	42 to 46	**DUAL:** Configuration pin, then possible user I/O	7 to 8	**VREF:** User I/O or input voltage reference for bank
0 to 2	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)
9	**N.C.:** Unconnected balls on the XC3S100E FPGA (◆)	16	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

TQ144: 144-lead Thin Quad Flat Package

The XC3S100E and the XC3S250E FPGAs are available in the 144-lead thin quad flat package, TQ144. Both devices share a common footprint for this package as shown in Table 134 and Figure 84.

Table 134 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The TQ144 package only supports 20 address output pins in the Byte-wide Peripheral Interface (BPI) configuration mode. In larger packages, there are 24 BPI address outputs.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at http://www.xilinx.com/bvdocs/publications/s3e_pin.zip.

Pinout Table

Table 134: **TQ144 Package Pinout**

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
0	IO	IO	P132	I/O
0	IO/VREF_0	IO/VREF_0	P124	VREF
0	IO_L01N_0	IO_L01N_0	P113	I/O
0	IO_L01P_0	IO_L01P_0	P112	I/O
0	IO_L02N_0	IO_L02N_0	P117	I/O
0	IO_L02P_0	IO_L02P_0	P116	I/O
0	IO_L04N_0/GCLK5	IO_L04N_0/GCLK5	P123	GCLK
0	IO_L04P_0/GCLK4	IO_L04P_0/GCLK4	P122	GCLK
0	IO_L05N_0/GCLK7	IO_L05N_0/GCLK7	P126	GCLK
0	IO_L05P_0/GCLK6	IO_L05P_0/GCLK6	P125	GCLK
0	IO_L07N_0/GCLK11	IO_L07N_0/GCLK11	P131	GCLK
0	IO_L07P_0/GCLK10	IO_L07P_0/GCLK10	P130	GCLK
0	IO_L08N_0/VREF_0	IO_L08N_0/VREF_0	P135	VREF
0	IO_L08P_0	IO_L08P_0	P134	I/O
0	IO_L09N_0	IO_L09N_0	P140	I/O
0	IO_L09P_0	IO_L09P_0	P139	I/O
0	IO_L10N_0/HSWAP	IO_L10N_0/HSWAP	P143	DUAL
0	IO_L10P_0	IO_L10P_0	P142	I/O
0	IP	IP	P111	INPUT
0	IP	IP	P114	INPUT
0	IP	IP	P136	INPUT
0	IP	IP	P141	INPUT
0	IP_L03N_0	IP_L03N_0	P120	INPUT
0	IP_L03P_0	IP_L03P_0	P119	INPUT
0	IP_L06N_0/GCLK9	IP_L06N_0/GCLK9	P129	GCLK
0	IP_L06P_0/GCLK8	IP_L06P_0/GCLK8	P128	GCLK
0	VCCO_0	VCCO_0	P121	VCCO
0	VCCO_0	VCCO_0	P138	VCCO
1	IO/A0	IO/A0	P98	DUAL
1	IO/VREF_1	IO/VREF_1	P83	VREF
1	IO_L01N_1/A15	IO_L01N_1/A15	P75	DUAL

Table 134: **TQ144 Package Pinout *(Continued)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
1	IO_L01P_1/A16	IO_L01P_1/A16	P74	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	P77	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	P76	DUAL
1	IO_L03N_1/A11	IO_L03N_1/A11	P82	DUAL
1	IO_L03P_1/A12	IO_L03P_1/A12	P81	DUAL
1	IO_L04N_1/A9/RHCLK1	IO_L04N_1/A9/RHCLK1	P86	RHCLK/DUAL
1	IO_L04P_1/A10/RHCLK0	IO_L04P_1/A10/RHCLK0	P85	RHCLK/DUAL
1	IO_L05N_1/A7/RHCLK3/TRDY1	IO_L05N_1/A7/RHCLK3	P88	RHCLK/DUAL
1	IO_L05P_1/A8/RHCLK2	IO_L05P_1/A8/RHCLK2	P87	RHCLK/DUAL
1	IO_L06N_1/A5/RHCLK5	IO_L06N_1/A5/RHCLK5	P92	RHCLK/DUAL
1	IO_L06P_1/A6/RHCLK4/IRDY1	IO_L06P_1/A6/RHCLK4	P91	RHCLK/DUAL
1	IO_L07N_1/A3/RHCLK7	IO_L07N_1/A3/RHCLK7	P94	RHCLK/DUAL
1	IO_L07P_1/A4/RHCLK6	IO_L07P_1/A4/RHCLK6	P93	RHCLK/DUAL
1	IO_L08N_1/A1	IO_L08N_1/A1	P97	DUAL
1	IO_L08P_1/A2	IO_L08P_1/A2	P96	DUAL
1	IO_L09N_1/LDC0	IO_L09N_1/LDC0	P104	DUAL
1	IO_L09P_1/HDC	IO_L09P_1/HDC	P103	DUAL
1	IO_L10N_1/LDC2	IO_L10N_1/LDC2	P106	DUAL
1	IO_L10P_1/LDC1	IO_L10P_1/LDC1	P105	DUAL
1	IP	IP	P78	INPUT
1	IP	IP	P84	INPUT
1	IP	IP	P89	INPUT
1	IP	IP	P101	INPUT
1	IP	IP	P107	INPUT
1	IP/VREF_1	IP/VREF_1	P95	VREF
1	VCCO_1	VCCO_1	P79	VCCO
1	VCCO_1	VCCO_1	P100	VCCO
2	IO/D5	IO/D5	P52	DUAL
2	IO/M1	IO/M1	P60	DUAL
2	IP/VREF_2	IO/VREF_2	P66	***100E:*** VREF(INPUT) ***250E:*** VREF(I/O)
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	P40	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	P39	DUAL
2	IO_L02N_2/MOSI/CSI_B	IO_L02N_2/MOSI/CSI_B	P44	DUAL
2	IO_L02P_2/DOUT/BUSY	IO_L02P_2/DOUT/BUSY	P43	DUAL
2	IO_L04N_2/D6/GCLK13	IO_L04N_2/D6/GCLK13	P51	DUAL/GCLK
2	IO_L04P_2/D7/GCLK12	IO_L04P_2/D7/GCLK12	P50	DUAL/GCLK
2	IO_L05N_2/D3/GCLK15	IO_L05N_2/D3/GCLK15	P54	DUAL/GCLK
2	IO_L05P_2/D4/GCLK14	IO_L05P_2/D4/GCLK14	P53	DUAL/GCLK
2	IO_L07N_2/D1/GCLK3	IO_L07N_2/D1/GCLK3	P59	DUAL/GCLK
2	IO_L07P_2/D2/GCLK2	IO_L07P_2/D2/GCLK2	P58	DUAL/GCLK
2	IO_L08N_2/DIN/D0	IO_L08N_2/DIN/D0	P63	DUAL

Table 134: **TQ144 Package Pinout *(Continued)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
2	IO_L08P_2/M0	IO_L08P_2/M0	P62	DUAL
2	IO_L09N_2/VS1/A18	IO_L09N_2/VS1/A18	P68	DUAL
2	IO_L09P_2/VS2/A19	IO_L09P_2/VS2/A19	P67	DUAL
2	IO_L10N_2/CCLK	IO_L10N_2/CCLK	P71	DUAL
2	IO_L10P_2/VS0/A17	IO_L10P_2/VS0/A17	P70	DUAL
2	IP	IP	P38	INPUT
2	IP	IP	P41	INPUT
2	IP	IP	P69	INPUT
2	IP_L03N_2/VREF_2	IP_L03N_2/VREF_2	P48	VREF
2	IP_L03P_2	IP_L03P_2	P47	INPUT
2	IP_L06N_2/M2/GCLK1	IP_L06N_2/M2/GCLK1	P57	DUAL/GCLK
2	IP_L06P_2/RDWR_B/GCLK0	IP_L06P_2/RDWR_B/GCLK0	P56	DUAL/GCLK
2	VCCO_2	VCCO_2	P42	VCCO
2	VCCO_2	VCCO_2	P49	VCCO
2	VCCO_2	VCCO_2	P64	VCCO
3	IP/VREF_3	IO/VREF_3	P31	***100E:*** VREF(INPUT) ***250E:*** VREF(I/O)
3	IO_L01N_3	IO_L01N_3	P3	I/O
3	IO_L01P_3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	P5	VREF
3	IO_L02P_3	IO_L02P_3	P4	I/O
3	IO_L03N_3	IO_L03N_3	P8	I/O
3	IO_L03P_3	IO_L03P_3	P7	I/O
3	IO_L04N_3/LHCLK1	IO_L04N_3/LHCLK1	P15	LHCLK
3	IO_L04P_3/LHCLK0	IO_L04P_3/LHCLK0	P14	LHCLK
3	IO_L05N_3/LHCLK3/IRDY2	IO_L05N_3/LHCLK3	P17	LHCLK
3	IO_L05P_3/LHCLK2	IO_L05P_3/LHCLK2	P16	LHCLK
3	IO_L06N_3/LHCLK5	IO_L06N_3/LHCLK5	P21	LHCLK
3	IO_L06P_3/LHCLK4/TRDY2	IO_L06P_3/LHCLK4	P20	LHCLK
3	IO_L07N_3/LHCLK7	IO_L07N_3/LHCLK7	P23	LHCLK
3	IO_L07P_3/LHCLK6	IO_L07P_3/LHCLK6	P22	LHCLK
3	IO_L08N_3	IO_L08N_3	P26	I/O
3	IO_L08P_3	IO_L08P_3	P25	I/O
3	IO_L09N_3	IO_L09N_3	P33	I/O
3	IO_L09P_3	IO_L09P_3	P32	I/O
3	IO_L10N_3	IO_L10N_3	P35	I/O
3	IO_L10P_3	IO_L10P_3	P34	I/O
3	IP	IP	P6	INPUT
3	IO	IP	P10	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P18	INPUT
3	IP	IP	P24	INPUT

Table 134: **TQ144 Package Pinout *(Continued)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
3	IO	IP	P29	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P36	INPUT
3	IP/VREF_3	IP/VREF_3	P12	VREF
3	VCCO_3	VCCO_3	P13	VCCO
3	VCCO_3	VCCO_3	P28	VCCO
GND	GND	GND	P11	GND
GND	GND	GND	P19	GND
GND	GND	GND	P27	GND
GND	GND	GND	P37	GND
GND	GND	GND	P46	GND
GND	GND	GND	P55	GND
GND	GND	GND	P61	GND
GND	GND	GND	P73	GND
GND	GND	GND	P90	GND
GND	GND	GND	P99	GND
GND	GND	GND	P118	GND
GND	GND	GND	P127	GND
GND	GND	GND	P133	GND
VCCAUX	DONE	DONE	P72	CONFIG
VCCAUX	PROG_B	PROG_B	P1	CONFIG
VCCAUX	TCK	TCK	P110	JTAG
VCCAUX	TDI	TDI	P144	JTAG
VCCAUX	TDO	TDO	P109	JTAG
VCCAUX	TMS	TMS	P108	JTAG
VCCAUX	VCCAUX	VCCAUX	P30	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P65	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P102	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P137	VCCAUX
VCCINT	VCCINT	VCCINT	P9	VCCINT
VCCINT	VCCINT	VCCINT	P45	VCCINT
VCCINT	VCCINT	VCCINT	P80	VCCINT
VCCINT	VCCINT	VCCINT	P115	VCCINT

User I/Os by Bank

Table 135 and Table 136 indicate how the 108 available user-I/O pins are distributed between the four I/O banks on the TQ144 package.

Table 135: **User I/Os Per Bank for the XC3S100E in the TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	26	9	6	1	2	8
Right	1	28	0	5	21	2	0(1)
Bottom	2	26	0	4	20	2	0(1)
Left	3	28	13	4	0	3	8
TOTAL		**108**	**22**	**19**	**42**	**9**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 136: **User I/Os Per Bank for the XC3S250E in TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	26	9	6	1	2	8
Right	1	28	0	5	21	2	0(1)
Bottom	2	26	0	4	20	2	0(1)
Left	3	28	11	6	0	3	8
TOTAL		**108**	**20**	**21**	**42**	**9**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

Table 137 summarizes any footprint and functionality differences between the XC3S100E and the XC3S250E FPGAs that may affect easy migration between devices. There are four such pins. All other pins not listed in Table 137 unconditionally migrate between Spartan-3E devices available in the TQ144 package.

The arrows indicate the direction for easy migration. For example, a left-facing arrow indicates that the pin on the XC3S250E unconditionally migrates to the pin on the XC3S100E. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 137: **TQ144 Footprint Migration Differences**

TQ144 Pin	Bank	XC3S100E Type	Migration	XC3S250E Type
P10	3	I/O	←	INPUT
P29	3	I/O	←	INPUT
P31	3	VREF(INPUT)	→	VREF(I/O)
P66	2	VREF(INPUT)	→	VREF(I/O)
DIFFERENCES			**4**	

Legend:

→	This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.
←	This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation. Double arrows (←→) indicates a pinout migration difference between the XC3S100E and XC3S250E.

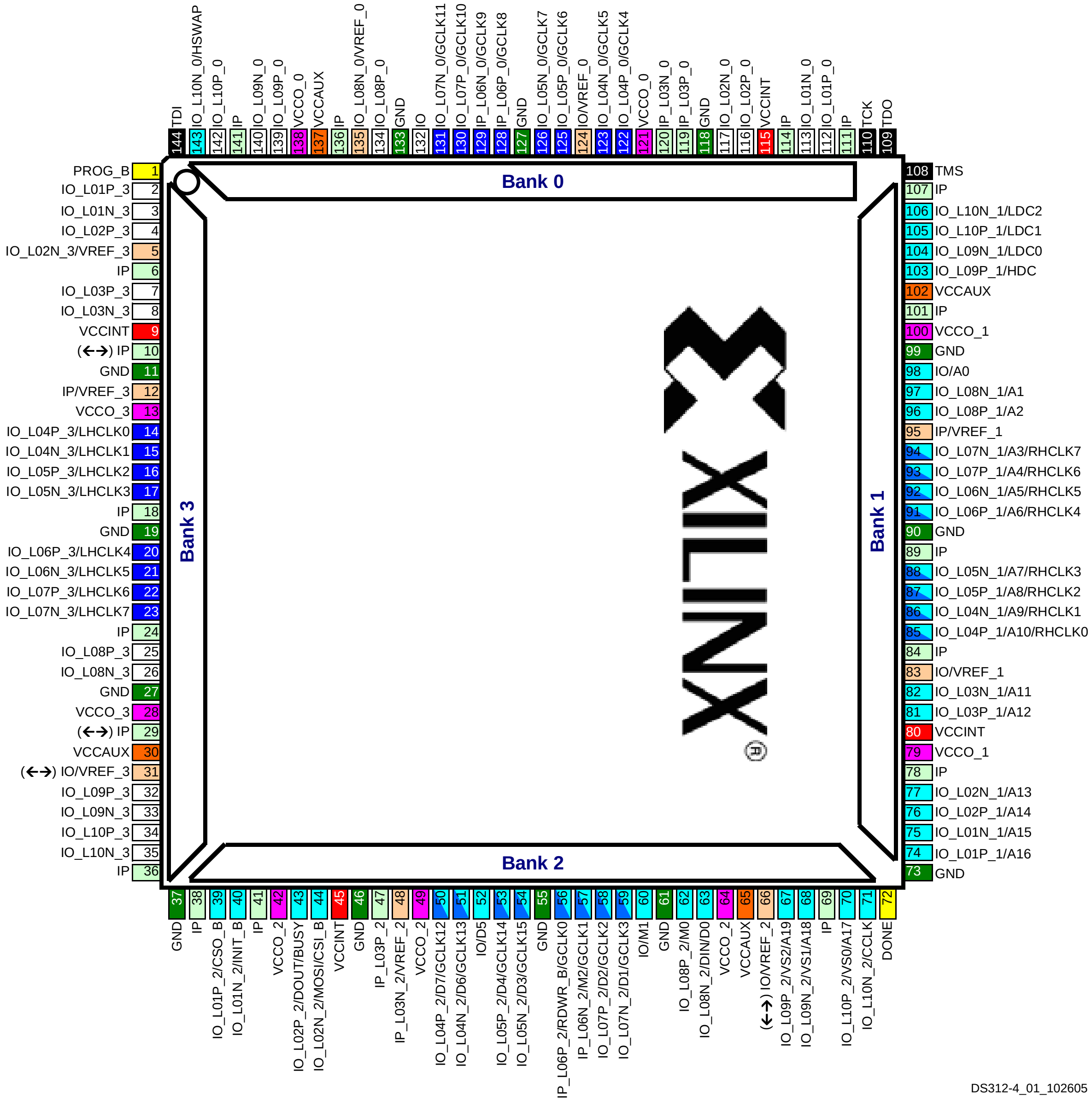


Figure 84: **TQ144 Package Footprint (top view)**

20	**I/O:** Unrestricted, general-purpose user I/O	42	**DUAL:** Configuration pin, then possible user I/O	9	**VREF:** User I/O or input voltage reference for bank
21	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	9	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

PQ208: 208-pin Plastic Quad Flat Package

The 208-pin plastic quad flat package, PQ208, supports two different Spartan-3E FPGAs, including the XC3S250E and the XC3S500E.

Table 138 lists all the PQ208 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3e_pin.zip.

Pinout Table

Table 138: **PQ208 Package Pinout**

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
0	IO	P187	I/O
0	IO/VREF_0	P179	VREF
0	IO_L01N_0	P161	I/O
0	IO_L01P_0	P160	I/O
0	IO_L02N_0/VREF_0	P163	VREF
0	IO_L02P_0	P162	I/O
0	IO_L03N_0	P165	I/O
0	IO_L03P_0	P164	I/O
0	IO_L04N_0/VREF_0	P168	VREF
0	IO_L04P_0	P167	I/O
0	IO_L05N_0	P172	I/O
0	IO_L05P_0	P171	I/O
0	IO_L07N_0/GCLK5	P178	GCLK
0	IO_L07P_0/GCLK4	P177	GCLK
0	IO_L08N_0/GCLK7	P181	GCLK
0	IO_L08P_0/GCLK6	P180	GCLK
0	IO_L10N_0/GCLK11	P186	GCLK
0	IO_L10P_0/GCLK10	P185	GCLK
0	IO_L11N_0	P190	I/O
0	IO_L11P_0	P189	I/O
0	IO_L12N_0/VREF_0	P193	VREF
0	IO_L12P_0	P192	I/O
0	IO_L13N_0	P197	I/O
0	IO_L13P_0	P196	I/O
0	IO_L14N_0/VREF_0	P200	VREF
0	IO_L14P_0	P199	I/O
0	IO_L15N_0	P203	I/O
0	IO_L15P_0	P202	I/O
0	IO_L16N_0/HSWAP	P206	DUAL
0	IO_L16P_0	P205	I/O
0	IP	P159	INPUT
0	IP	P169	INPUT
0	IP	P194	INPUT
0	IP	P204	INPUT
0	IP_L06N_0	P175	INPUT
0	IP_L06P_0	P174	INPUT
0	IP_L09N_0/GCLK9	P184	GCLK
0	IP_L09P_0/GCLK8	P183	GCLK
0	VCCO_0	P176	VCCO
0	VCCO_0	P191	VCCO
0	VCCO_0	P201	VCCO
1	IO_L01N_1/A15	P107	DUAL
1	IO_L01P_1/A16	P106	DUAL
1	IO_L02N_1/A13	P109	DUAL
1	IO_L02P_1/A14	P108	DUAL
1	IO_L03N_1/VREF_1	P113	VREF
1	IO_L03P_1	P112	I/O
1	IO_L04N_1	P116	I/O
1	IO_L04P_1	P115	I/O
1	IO_L05N_1/A11	P120	DUAL
1	IO_L05P_1/A12	P119	DUAL
1	IO_L06N_1/VREF_1	P123	VREF
1	IO_L06P_1	P122	I/O
1	IO_L07N_1/A9/RHCLK1	P127	RHCLK/DUAL
1	IO_L07P_1/A10/RHCLK0	P126	RHCLK/DUAL
1	IO_L08N_1/A7/RHCLK3	P129	RHCLK/DUAL
1	IO_L08P_1/A8/RHCLK2	P128	RHCLK/DUAL
1	IO_L09N_1/A5/RHCLK5	P133	RHCLK/DUAL
1	IO_L09P_1/A6/RHCLK4	P132	RHCLK/DUAL
1	IO_L10N_1/A3/RHCLK7	P135	RHCLK/DUAL
1	IO_L10P_1/A4/RHCLK6	P134	RHCLK/DUAL
1	IO_L11N_1/A1	P138	DUAL
1	IO_L11P_1/A2	P137	DUAL
1	IO_L12N_1/A0	P140	DUAL
1	IO_L12P_1	P139	I/O
1	IO_L13N_1	P145	I/O
1	IO_L13P_1	P144	I/O

Table 138: **PQ208 Package Pinout *(Continued)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
1	IO_L14N_1	P147	I/O
1	IO_L14P_1	P146	I/O
1	IO_L15N_1/LDC0	P151	DUAL
1	IO_L15P_1/HDC	P150	DUAL
1	IO_L16N_1/LDC2	P153	DUAL
1	IO_L16P_1/LDC1	P152	DUAL
1	IP	P110	INPUT
1	IP	P118	INPUT
1	IP	P124	INPUT
1	IP	P130	INPUT
1	IP	P142	INPUT
1	IP	P148	INPUT
1	IP	P154	INPUT
1	IP/VREF_1	P136	VREF
1	VCCO_1	P114	VCCO
1	VCCO_1	P125	VCCO
1	VCCO_1	P143	VCCO
2	IO/D5	P76	DUAL
2	IO/M1	P84	DUAL
2	IO/VREF_2	P98	VREF
2	IO_L01N_2/INIT_B	P56	DUAL
2	IO_L01P_2/CSO_B	P55	DUAL
2	IO_L03N_2/MOSI/CSI_B	P61	DUAL
2	IO_L03P_2/DOUT/BUSY	P60	DUAL
2	IO_L04N_2	P63	I/O
2	IO_L04P_2	P62	I/O
2	IO_L05N_2	P65	I/O
2	IO_L05P_2	P64	I/O
2	IO_L06N_2	P69	I/O
2	IO_L06P_2	P68	I/O
2	IO_L08N_2/D6/GCLK13	P75	DUAL/GCLK
2	IO_L08P_2/D7/GCLK12	P74	DUAL/GCLK
2	IO_L09N_2/D3/GCLK15	P78	DUAL/GCLK
2	IO_L09P_2/D4/GCLK14	P77	DUAL/GCLK
2	IO_L11N_2/D1/GCLK3	P83	DUAL/GCLK
2	IO_L11P_2/D2/GCLK2	P82	DUAL/GCLK
2	IO_L12N_2/DIN/D0	P87	DUAL
2	IO_L12P_2/M0	P86	DUAL
2	IO_L13N_2	P90	I/O
2	IO_L13P_2	P89	I/O

Table 138: **PQ208 Package Pinout *(Continued)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
2	IO_L14N_2/A22	P94	DUAL
2	IO_L14P_2/A23	P93	DUAL
2	IO_L15N_2/A20	P97	DUAL
2	IO_L15P_2/A21	P96	DUAL
2	IO_L16N_2/VS1/A18	P100	DUAL
2	IO_L16P_2/VS2/A19	P99	DUAL
2	IO_L17N_2/CCLK	P103	DUAL
2	IO_L17P_2/VS0/A17	P102	DUAL
2	IP	P54	INPUT
2	IP	P91	INPUT
2	IP	P101	INPUT
2	IP_L02N_2	P58	INPUT
2	IP_L02P_2	P57	INPUT
2	IP_L07N_2/VREF_2	P72	VREF
2	IP_L07P_2	P71	INPUT
2	IP_L10N_2/M2/GCLK1	P81	DUAL/GCLK
2	IP_L10P_2/RDWR_B/ GCLK0	P80	DUAL/GCLK
2	VCCO_2	P59	VCCO
2	VCCO_2	P73	VCCO
2	VCCO_2	P88	VCCO
3	IO/VREF_3	P45	VREF
3	IO_L01N_3	P3	I/O
3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	P5	VREF
3	IO_L02P_3	P4	I/O
3	IO_L03N_3	P9	I/O
3	IO_L03P_3	P8	I/O
3	IO_L04N_3	P12	I/O
3	IO_L04P_3	P11	I/O
3	IO_L05N_3	P16	I/O
3	IO_L05P_3	P15	I/O
3	IO_L06N_3	P19	I/O
3	IO_L06P_3	P18	I/O
3	IO_L07N_3/LHCLK1	P23	LHCLK
3	IO_L07P_3/LHCLK0	P22	LHCLK
3	IO_L08N_3/LHCLK3	P25	LHCLK
3	IO_L08P_3/LHCLK2	P24	LHCLK
3	IO_L09N_3/LHCLK5	P29	LHCLK
3	IO_L09P_3/LHCLK4	P28	LHCLK
3	IO_L10N_3/LHCLK7	P31	LHCLK

Table 138: **PQ208 Package Pinout *(Continued)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
3	IO_L10P_3/LHCLK6	P30	LHCLK
3	IO_L11N_3	P34	I/O
3	IO_L11P_3	P33	I/O
3	IO_L12N_3	P36	I/O
3	IO_L12P_3	P35	I/O
3	IO_L13N_3	P40	I/O
3	IO_L13P_3	P39	I/O
3	IO_L14N_3	P42	I/O
3	IO_L14P_3	P41	I/O
3	IO_L15N_3	P48	I/O
3	IO_L15P_3	P47	I/O
3	IO_L16N_3	P50	I/O
3	IO_L16P_3	P49	I/O
3	IP	P6	INPUT
3	IP	P14	INPUT
3	IP	P26	INPUT
3	IP	P32	INPUT
3	IP	P43	INPUT
3	IP	P51	INPUT
3	IP/VREF_3	P20	VREF
3	VCCO_3	P21	VCCO
3	VCCO_3	P38	VCCO
3	VCCO_3	P46	VCCO
GND	GND	P10	GND
GND	GND	P17	GND
GND	GND	P27	GND
GND	GND	P37	GND
GND	GND	P52	GND
GND	GND	P53	GND
GND	GND	P70	GND
GND	GND	P79	GND
GND	GND	P85	GND
GND	GND	P95	GND
GND	GND	P105	GND
GND	GND	P121	GND
GND	GND	P131	GND
GND	GND	P141	GND
GND	GND	P156	GND
GND	GND	P173	GND
GND	GND	P182	GND

Table 138: **PQ208 Package Pinout *(Continued)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
GND	GND	P188	GND
GND	GND	P198	GND
GND	GND	P208	GND
VCCAUX	DONE	P104	CONFIG
VCCAUX	PROG_B	P1	CONFIG
VCCAUX	TCK	P158	JTAG
VCCAUX	TDI	P207	JTAG
VCCAUX	TDO	P157	JTAG
VCCAUX	TMS	P155	JTAG
VCCAUX	VCCAUX	P7	VCCAUX
VCCAUX	VCCAUX	P44	VCCAUX
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P92	VCCAUX
VCCAUX	VCCAUX	P111	VCCAUX
VCCAUX	VCCAUX	P149	VCCAUX
VCCAUX	VCCAUX	P166	VCCAUX
VCCAUX	VCCAUX	P195	VCCAUX
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P67	VCCINT
VCCINT	VCCINT	P117	VCCINT
VCCINT	VCCINT	P170	VCCINT

User I/Os by Bank

Table 139 indicates how the 158 available user-I/O pins are distributed between the four I/O banks on the PQ208 package.

Footprint Migration Differences

The XC3S250E and XC3S500E FPGAs have identical footprints in the PQ208 package. Designs can migrate between the XC3S250E and XC3S500E without further consideration.

Table 139: **User I/Os Per Bank for the XC3S250E and XC3S500E in the PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	38	18	6	1	5	8
Right	1	40	9	7	21	3	0(1)
Bottom	2	40	8	6	24	2	0(1)
Left	3	40	23	6	0	3	8
TOTAL		**158**	**58**	**25**	**46**	**13**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

PQ208 Footprint (Left)

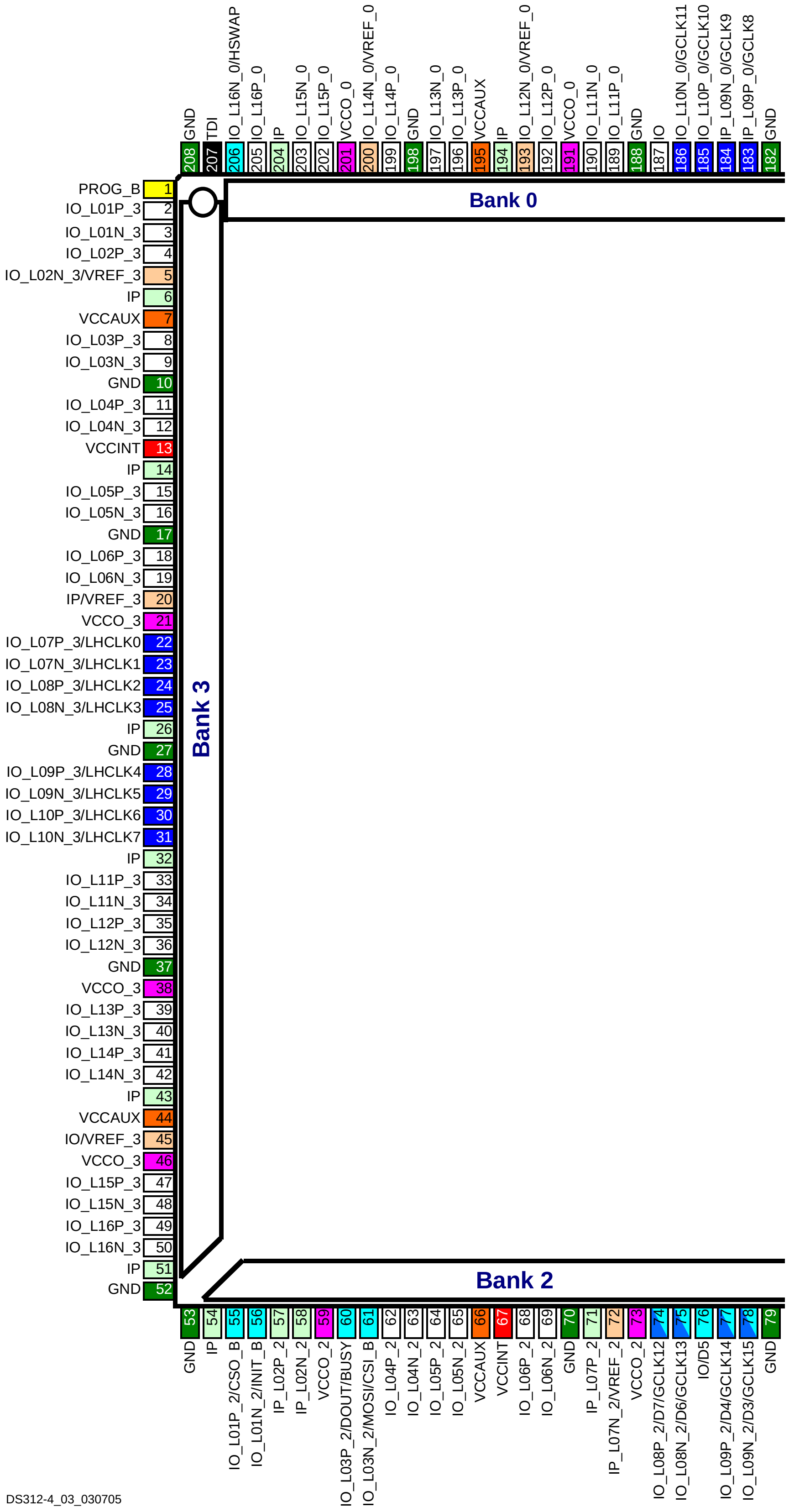


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Figure 85: **PQ208 Footprint (Left)**

PQ208 Footprint (Right)

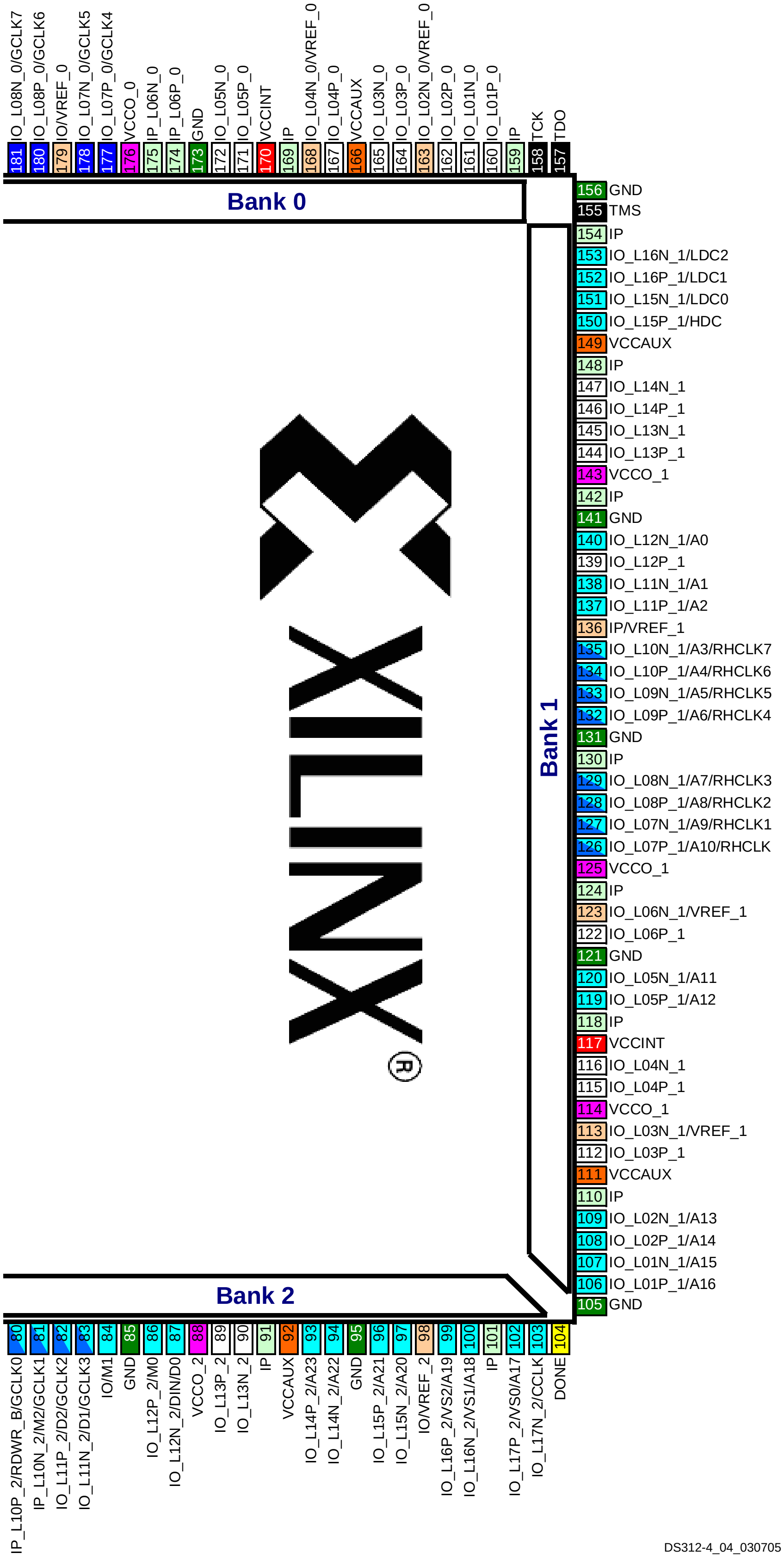

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Figure 86: **PQ208 Footprint (Right)**

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports three different Spartan-3E FPGAs, including the XC3S250E, the XC3S500E, and the XC3S1200E.

Table 140 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs. The XC3S250E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 140 and with the black diamond character (◆) in Table 140 and Figure 87.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S250E FPGA maps to a VREF pin on the XC3S500E and XC3S1200E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S250E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 144 summarizes the Spartan-3E footprint migration differences for the FT256 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at http://www.xilinx.com/bvdocs/publications/s3e_pin.zip.

Pinout Table

Table 140: **FT256 Package Pinout**

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO	IO	IO	A7	I/O
0	IO	IO	IO	A12	I/O
0	IO	IO	IO	B4	I/O
0	IP	IP	IO	B6	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IP	IP	IO	B10	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	D9	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A14	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B14	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	A13	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	B13	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	E11	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	D11	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B11	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	C11	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E10	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	D10	I/O
0	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	F9	GCLK
0	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	E9	GCLK
0	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	A9	GCLK
0	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	A10	GCLK
0	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	D8	GCLK
0	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	C8	GCLK

Table 140: **FT256 Package Pinout *(Continued)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO_L12N_0	IO_L12N_0	IO_L12N_0	F8	I/O
0	IO_L12P_0	IO_L12P_0	IO_L12P_0	E8	I/O
0	N.C. (◆)	IO_L13N_0	IO_L13N_0	C7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
0	N.C. (◆)	IO_L13P_0	IO_L13P_0	B7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
0	IO_L14N_0/VREF_0	IO_L14N_0/VREF_0	IO_L14N_0/VREF_0	D7	VREF
0	IO_L14P_0	IO_L14P_0	IO_L14P_0	E7	I/O
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	D6	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	C6	I/O
0	IO_L17N_0/VREF_0	IO_L17N_0/VREF_0	IO_L17N_0/VREF_0	A4	VREF
0	IO_L17P_0	IO_L17P_0	IO_L17P_0	A5	I/O
0	IO_L18N_0	IO_L18N_0	IO_L18N_0	C4	I/O
0	IO_L18P_0	IO_L18P_0	IO_L18P_0	C5	I/O
0	IO_L19N_0/HSWAP	IO_L19N_0/HSWAP	IO_L19N_0/HSWAP	B3	DUAL
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	C3	I/O
0	IP	IP	IP	A3	INPUT
0	IP	IP	IP	C13	INPUT
0	IP_L02N_0	IP_L02N_0	IP_L02N_0	C12	INPUT
0	IP_L02P_0	IP_L02P_0	IP_L02P_0	D12	INPUT
0	IP_L07N_0	IP_L07N_0	IP_L07N_0	C9	INPUT
0	IP_L07P_0	IP_L07P_0	IP_L07P_0	C10	INPUT
0	IP_L10N_0/GCLK9	IP_L10N_0/GCLK9	IP_L10N_0/GCLK9	B8	GCLK
0	IP_L10P_0/GCLK8	IP_L10P_0/GCLK8	IP_L10P_0/GCLK8	A8	GCLK
0	IP_L16N_0	IP_L16N_0	IP_L16N_0	E6	INPUT
0	IP_L16P_0	IP_L16P_0	IP_L16P_0	D5	INPUT
0	VCCO_0	VCCO_0	VCCO_0	B5	VCCO
0	VCCO_0	VCCO_0	VCCO_0	B12	VCCO
0	VCCO_0	VCCO_0	VCCO_0	F7	VCCO
0	VCCO_0	VCCO_0	VCCO_0	F10	VCCO
1	IO_L01N_1/A15	IO_L01N_1/A15	IO_L01N_1/A15	R15	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	IO_L01P_1/A16	R16	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	IO_L02N_1/A13	P15	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	IO_L02P_1/A14	P16	DUAL
1	N.C. (◆)	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	N15	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
1	N.C. (◆)	IO_L03P_1	IO_L03P_1	N14	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O

Table 140: **FT256 Package Pinout** ***(Continued)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
1	IO_L04N_1/VREF_1	IO_L04N_1/VREF_1	IO_L04N_1/VREF_1	M16	VREF
1	IO_L04P_1	IO_L04P_1	IO_L04P_1	N16	I/O
1	N.C. (◆)	IO_L05N_1	IO_L05N_1	L13	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	N.C. (◆)	IO_L05P_1	IO_L05P_1	L12	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	IO_L06N_1	IO_L06N_1	IO_L06N_1	L15	I/O
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	L14	I/O
1	IO_L07N_1/A11	IO_L07N_1/A11	IO_L07N_1/A11	K12	DUAL
1	IO_L07P_1/A12	IO_L07P_1/A12	IO_L07P_1/A12	K13	DUAL
1	IO_L08N_1/VREF_1	IO_L08N_1/VREF_1	IO_L08N_1/VREF_1	K14	VREF
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	K15	I/O
1	IO_L09N_1/A9/RHCLK1	IO_L09N_1/A9/RHCLK1	IO_L09N_1/A9/RHCLK1	J16	RHCLK/DUAL
1	IO_L09P_1/A10/RHCLK0	IO_L09P_1/A10/RHCLK0	IO_L09P_1/A10/RHCLK0	K16	RHCLK/DUAL
1	IO_L10N_1/A7/RHCLK3/ TRDY1	IO_L10N_1/A7/RHCLK3/ TRDY1	IO_L10N_1/A7/RHCLK3/ TRDY1	J13	RHCLK/DUAL
1	IO_L10P_1/A8/RHCLK2	IO_L10P_1/A8/RHCLK2	IO_L10P_1/A8/RHCLK2	J14	RHCLK/DUAL
1	IO_L11N_1/A5/RHCLK5	IO_L11N_1/A5/RHCLK5	IO_L11N_1/A5/RHCLK5	H14	RHCLK/DUAL
1	IO_L11P_1/A6/RHCLK4/ IRDY1	IO_L11P_1/A6/RHCLK4/ IRDY1	IO_L11P_1/A6/RHCLK4/ IRDY1	H15	RHCLK/DUAL
1	IO_L12N_1/A3/RHCLK7	IO_L12N_1/A3/RHCLK7	IO_L12N_1/A3/RHCLK7	H11	RHCLK/DUAL
1	IO_L12P_1/A4/RHCLK6	IO_L12P_1/A4/RHCLK6	IO_L12P_1/A4/RHCLK6	H12	RHCLK/DUAL
1	IO_L13N_1/A1	IO_L13N_1/A1	IO_L13N_1/A1	G16	DUAL
1	IO_L13P_1/A2	IO_L13P_1/A2	IO_L13P_1/A2	G15	DUAL
1	IO_L14N_1/A0	IO_L14N_1/A0	IO_L14N_1/A0	G14	DUAL
1	IO_L14P_1	IO_L14P_1	IO_L14P_1	G13	I/O
1	IO_L15N_1	IO_L15N_1	IO_L15N_1	F15	I/O
1	IO_L15P_1	IO_L15P_1	IO_L15P_1	F14	I/O
1	IO_L16N_1	IO_L16N_1	IO_L16N_1	F12	I/O
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	F13	I/O
1	N.C. (◆)	IO_L17N_1	IO_L17N_1	E16	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	N.C. (◆).	IO_L17P_1	IO_L17P_1	E13	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	IO_L18N_1/LDC0	IO_L18N_1/LDC0	IO_L18N_1/LDC0	D14	DUAL
1	IO_L18P_1/HDC	IO_L18P_1/HDC	IO_L18P_1/HDC	D15	DUAL
1	IO_L19N_1/LDC2	IO_L19N_1/LDC2	IO_L19N_1/LDC2	C15	DUAL
1	IO_L19P_1/LDC1	IO_L19P_1/LDC1	IO_L19P_1/LDC1	C16	DUAL

Table 140: **FT256 Package Pinout *(Continued)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
1	IP	IP	IP	B16	INPUT
1	IP	IP	IP	E14	INPUT
1	IP	IP	IP	G12	INPUT
1	IP	IP	IP	H16	INPUT
1	IP	IP	IP	J11	INPUT
1	IP	IP	IP	J12	INPUT
1	IP	IP	IP	M13	INPUT
1	IO	IO	IP	M14	***250E:*** I/O ***500E:*** I/O ***1200E:*** INPUT
1	IO/VREF_1	IP/VREF_1	IP/VREF_1	D16	***250E:*** VREF(I/O) ***500E:*** VREF(INPUT) ***1200E:*** VREF(INPUT)
1	IP/VREF_1	IP/VREF_1	IP/VREF_1	H13	VREF
1	VCCO_1	VCCO_1	VCCO_1	E15	VCCO
1	VCCO_1	VCCO_1	VCCO_1	G11	VCCO
1	VCCO_1	VCCO_1	VCCO_1	K11	VCCO
1	VCCO_1	VCCO_1	VCCO_1	M15	VCCO
2	IP	IP	IO	M7	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
2	IP	IP	IO	T12	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
2	IO/D5	IO/D5	IO/D5	T8	DUAL
2	IO/M1	IO/M1	IO/M1	T10	DUAL
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	P13	VREF
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	R4	VREF
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	P4	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	P3	DUAL
2	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	N5	DUAL
2	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	P5	DUAL
2	IO_L04N_2	IO_L04N_2	IO_L04N_2	T5	I/O
2	IO_L04P_2	IO_L04P_2	IO_L04P_2	T4	I/O
2	IO_L05N_2	IO_L05N_2	IO_L05N_2	N6	I/O
2	IO_L05P_2	IO_L05P_2	IO_L05P_2	M6	I/O
2	IO_L06N_2	IO_L06N_2	IO_L06N_2	P6	I/O
2	IO_L06P_2	IO_L06P_2	IO_L06P_2	R6	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	P7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O

Table 140: **FT256 Package Pinout *(Continued)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	N7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
2	IO_L09N_2/D6/GCLK13	IO_L09N_2/D6/GCLK13	IO_L09N_2/D6/GCLK13	L8	DUAL/GCLK
2	IO_L09P_2/D7/GCLK12	IO_L09P_2/D7/GCLK12	IO_L09P_2/D7/GCLK12	M8	DUAL/GCLK
2	IO_L10N_2/D3/GCLK15	IO_L10N_2/D3/GCLK15	IO_L10N_2/D3/GCLK15	P8	DUAL/GCLK
2	IO_L10P_2/D4/GCLK14	IO_L10P_2/D4/GCLK14	IO_L10P_2/D4/GCLK14	N8	DUAL/GCLK
2	IO_L12N_2/D1/GCLK3	IO_L12N_2/D1/GCLK3	IO_L12N_2/D1/GCLK3	N9	DUAL/GCLK
2	IO_L12P_2/D2/GCLK2	IO_L12P_2/D2/GCLK2	IO_L12P_2/D2/GCLK2	P9	DUAL/GCLK
2	IO_L13N_2/DIN/D0	IO_L13N_2/DIN/D0	IO_L13N_2/DIN/D0	M9	DUAL
2	IO_L13P_2/M0	IO_L13P_2/M0	IO_L13P_2/M0	L9	DUAL
2	N.C. (◆)	IO_L14N_2/VREF_2	IO_L14N_2/VREF_2	R10	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
2	N.C. (◆)	IO_L14P_2	IO_L14P_2	P10	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
2	IO_L15N_2	IO_L15N_2	IO_L15N_2	M10	I/O
2	IO_L15P_2	IO_L15P_2	IO_L15P_2	N10	I/O
2	IO_L16N_2/A22	IO_L16N_2/A22	IO_L16N_2/A22	P11	DUAL
2	IO_L16P_2/A23	IO_L16P_2/A23	IO_L16P_2/A23	R11	DUAL
2	IO_L18N_2/A20	IO_L18N_2/A20	IO_L18N_2/A20	N12	DUAL
2	IO_L18P_2/A21	IO_L18P_2/A21	IO_L18P_2/A21	P12	DUAL
2	IO_L19N_2/VS1/A18	IO_L19N_2/VS1/A18	IO_L19N_2/VS1/A18	R13	DUAL
2	IO_L19P_2/VS2/A19	IO_L19P_2/VS2/A19	IO_L19P_2/VS2/A19	T13	DUAL
2	IO_L20N_2/CCLK	IO_L20N_2/CCLK	IO_L20N_2/CCLK	R14	DUAL
2	IO_L20P_2/VS0/A17	IO_L20P_2/VS0/A17	IO_L20P_2/VS0/A17	P14	DUAL
2	IP	IP	IP	T2	INPUT
2	IP	IP	IP	T14	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	R3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	T3	INPUT
2	IP_L08N_2/VREF_2	IP_L08N_2/VREF_2	IP_L08N_2/VREF_2	T7	VREF
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	R7	INPUT
2	IP_L11N_2/M2/GCLK1	IP_L11N_2/M2/GCLK1	IP_L11N_2/M2/GCLK1	R9	DUAL/GCLK
2	IP_L11P_2/RDWR_B/ GCLK0	IP_L11P_2/RDWR_B/ GCLK0	IP_L11P_2/RDWR_B/ GCLK0	T9	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	M11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	N11	INPUT
2	VCCO_2	VCCO_2	VCCO_2	L7	VCCO
2	VCCO_2	VCCO_2	VCCO_2	L10	VCCO
2	VCCO_2	VCCO_2	VCCO_2	R5	VCCO
2	VCCO_2	VCCO_2	VCCO_2	R12	VCCO

Table 140: **FT256 Package Pinout *(Continued)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	B2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	B1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	C2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	C1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E4	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E3	I/O
3	N.C. (◆)	IO_L04N_3/VREF_3	IO_L04N_3/VREF_3	F4	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
3	N.C. (◆)	IO_L04P_3	IO_L04P_3	F3	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L05N_3	IO_L05N_3	IO_L05N_3	E1	I/O
3	IO_L05P_3	IO_L05P_3	IO_L05P_3	D1	I/O
3	IO_L06N_3	IO_L06N_3	IO_L06N_3	G4	I/O
3	IO_L06P_3	IO_L06P_3	IO_L06P_3	G5	I/O
3	IO_L07N_3	IO_L07N_3	IO_L07N_3	G2	I/O
3	IO_L07P_3	IO_L07P_3	IO_L07P_3	G3	I/O
3	IO_L08N_3/LHCLK1	IO_L08N_3/LHCLK1	IO_L08N_3/LHCLK1	H6	LHCLK
3	IO_L08P_3/LHCLK0	IO_L08P_3/LHCLK0	IO_L08P_3/LHCLK0	H5	LHCLK
3	IO_L09N_3/LHCLK3/ IRDY2	IO_L09N_3/LHCLK3/ IRDY2	IO_L09N_3/LHCLK3/ IRDY2	H4	LHCLK
3	IO_L09P_3/LHCLK2	IO_L09P_3/LHCLK2	IO_L09P_3/LHCLK2	H3	LHCLK
3	IO_L10N_3/LHCLK5	IO_L10N_3/LHCLK5	IO_L10N_3/LHCLK5	J3	LHCLK
3	IO_L10P_3/LHCLK4/ TRDY2	IO_L10P_3/LHCLK4/ TRDY2	IO_L10P_3/LHCLK4/ TRDY2	J2	LHCLK
3	IO_L11N_3/LHCLK7	IO_L11N_3/LHCLK7	IO_L11N_3/LHCLK7	J4	LHCLK
3	IO_L11P_3/LHCLK6	IO_L11P_3/LHCLK6	IO_L11P_3/LHCLK6	J5	LHCLK
3	IO_L12N_3	IO_L12N_3	IO_L12N_3	K1	I/O
3	IO_L12P_3	IO_L12P_3	IO_L12P_3	J1	I/O
3	IO_L13N_3	IO_L13N_3	IO_L13N_3	K3	I/O
3	IO_L13P_3	IO_L13P_3	IO_L13P_3	K2	I/O
3	N.C. (◆)	IO_L14N_3/VREF_3	IO_L14N_3/VREF_3	L2	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
3	N.C. (◆)	IO_L14P_3	IO_L14P_3	L3	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L15N_3	IO_L15N_3	IO_L15N_3	L5	I/O
3	IO_L15P_3	IO_L15P_3	IO_L15P_3	K5	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	N1	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	M1	I/O

Table 140: **FT256 Package Pinout *(Continued)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
3	N.C. (◆)	IO_L17N_3	IO_L17N_3	L4	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	N.C. (◆)	IO_L17P_3	IO_L17P_3	M4	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L18N_3	IO_L18N_3	IO_L18N_3	P1	I/O
3	IO_L18P_3	IO_L18P_3	IO_L18P_3	P2	I/O
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	R1	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	R2	I/O
3	IP	IP	IP	D2	INPUT
3	IP	IP	IP	F2	INPUT
3	IO	IO	IP	F5	***250E:*** I/O ***500E:*** I/O ***1200E:*** INPUT
3	IP	IP	IP	H1	INPUT
3	IP	IP	IP	J6	INPUT
3	IP	IP	IP	K4	INPUT
3	IP	IP	IP	M3	INPUT
3	IP	IP	IP	N3	INPUT
3	IP/VREF_3	IP/VREF_3	IP/VREF_3	G1	VREF
3	IO/VREF_3	IO/VREF_3	IP/VREF_3	N2	***250E:*** VREF(I/O) ***500E:*** VREF(I/O) ***1200E:*** VREF(INPUT)
3	VCCO_3	VCCO_3	VCCO_3	E2	VCCO
3	VCCO_3	VCCO_3	VCCO_3	G6	VCCO
3	VCCO_3	VCCO_3	VCCO_3	K6	VCCO
3	VCCO_3	VCCO_3	VCCO_3	M2	VCCO
GND	GND	GND	GND	A1	GND
GND	GND	GND	GND	A16	GND
GND	GND	GND	GND	B9	GND
GND	GND	GND	GND	F6	GND
GND	GND	GND	GND	F11	GND
GND	GND	GND	GND	G7	GND
GND	GND	GND	GND	G8	GND
GND	GND	GND	GND	G9	GND
GND	GND	GND	GND	G10	GND
GND	GND	GND	GND	H2	GND
GND	GND	GND	GND	H7	GND
GND	GND	GND	GND	H8	GND
GND	GND	GND	GND	H9	GND

Table 140: **FT256 Package Pinout *(Continued)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
GND	GND	GND	GND	H10	GND
GND	GND	GND	GND	J7	GND
GND	GND	GND	GND	J8	GND
GND	GND	GND	GND	J9	GND
GND	GND	GND	GND	J10	GND
GND	GND	GND	GND	J15	GND
GND	GND	GND	GND	K7	GND
GND	GND	GND	GND	K8	GND
GND	GND	GND	GND	K9	GND
GND	GND	GND	GND	K10	GND
GND	GND	GND	GND	L6	GND
GND	GND	GND	GND	L11	GND
GND	GND	GND	GND	R8	GND
GND	GND	GND	GND	T1	GND
GND	GND	GND	GND	T16	GND
VCCAUX	DONE	DONE	DONE	T15	CONFIG
VCCAUX	PROG_B	PROG_B	PROG_B	D3	CONFIG
VCCAUX	TCK	TCK	TCK	A15	JTAG
VCCAUX	TDI	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	TDO	C14	JTAG
VCCAUX	TMS	TMS	TMS	B15	JTAG
VCCAUX	VCCAUX	VCCAUX	VCCAUX	A6	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	A11	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	F1	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	F16	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	L1	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	L16	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	T6	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	T11	VCCAUX
VCCINT	VCCINT	VCCINT	VCCINT	D4	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	D13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	E5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	E12	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	M5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	M12	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N4	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N13	VCCINT

User I/Os by Bank

Table 141, Table 142, and Table 143 indicate how the available user-I/O pins are distributed between the four I/O banks on the FT256 package.

The XC3S250E FPGA in the FT256 package has 18 unconnected balls, labeled with an "N.C." type. These pins are also indicated with the black diamond (◆) symbol in Figure 87.

Table 141: **User I/Os Per Bank on XC3S250E in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	44	20	10	1	5	8
Right	1	42	10	7	21	4	0(1)
Bottom	2	44	8	9	24	3	0(1)
Left	3	42	24	7	0	3	8
TOTAL		**172**	**62**	**33**	**46**	**15**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 142: **User I/Os Per Bank on XC3S500E in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	46	22	10	1	5	8
Right	1	48	15	7	21	5	0(1)
Bottom	2	48	11	9	24	4	0(1)
Left	3	48	28	7	0	5	8
TOTAL		**190**	**76**	**33**	**46**	**19**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 143: **User I/Os Per Bank on XC3S1200E in the FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	46	24	8	1	5	8
Right	1	48	14	8	21	5	0(1)
Bottom	2	48	13	7	24	4	0(1)
Left	3	48	27	8	0	5	8
TOTAL		**190**	**78**	**31**	**46**	**19**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

Table 144 summarizes any footprint and functionality differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs that may affect easy migration between devices in the FG256 package. There are 26 such balls. All other pins not listed in Table 144 unconditionally migrate between Spartan-3E devices available in the FT256 package.

The XC3S250E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S500E and the XC3S1200E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

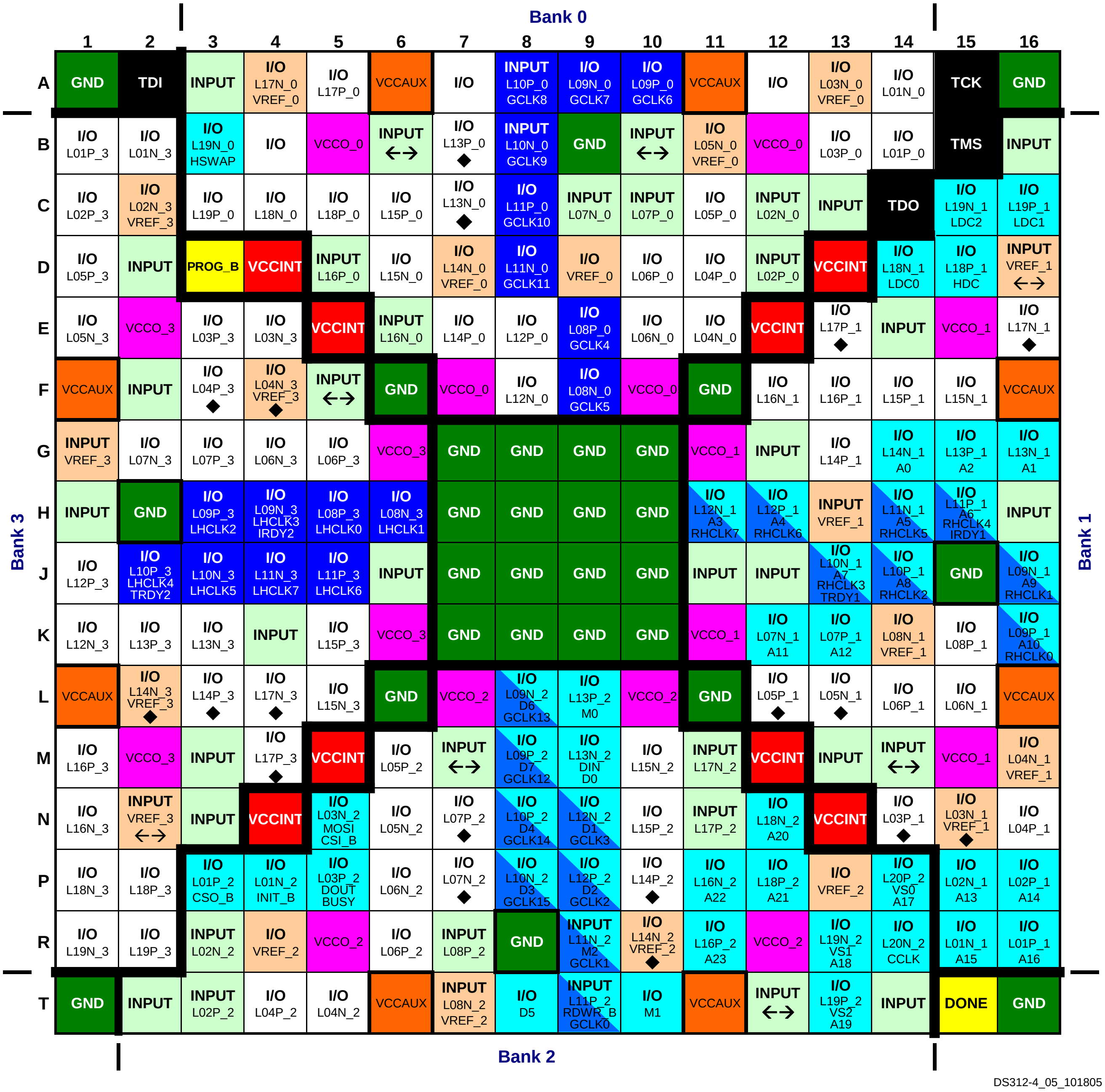
Table 144: **FT256 Footprint Migration Differences**

FT256 Ball	Bank	XC3S250E Type	Migration	XC3S500E Type	Migration	XC3S1200E Type	Migration	XC3S250E Type
B6	0	INPUT	←→	INPUT	→	I/O	←	INPUT
B7	0	N.C.	→	I/O	←→	I/O	←	N.C.
B10	0	INPUT	←→	INPUT	→	I/O	←	INPUT
C7	0	N.C.	→	I/O	←→	I/O	←	N.C.
D16	1	VREF(I/O)	←	VREF(INPUT)	←→	VREF(INPUT)	→	VREF(I/O)
E13	1	N.C.	→	I/O	←→	I/O	←	N.C.
E16	1	N.C.	→	I/O	←→	I/O	←	N.C.
F3	3	N.C.	→	I/O	←→	I/O	←	N.C.
F4	3	N.C.	→	VREF	←→	VREF	←	N.C.
F5	3	I/O	←→	I/O	←	INPUT	→	I/O
L2	3	N.C.	→	VREF	←→	VREF	←	N.C.
L3	3	N.C.	→	I/O	←→	I/O	←	N.C.
L4	3	N.C.	→	I/O	←→	I/O	←	N.C.
L12	1	N.C.	→	I/O	←→	I/O	←	N.C.
L13	1	N.C.	→	I/O	←→	I/O	←	N.C.
M4	3	N.C.	→	I/O	←→	I/O	←	N.C.
M7	2	INPUT	←→	INPUT	→	I/O	←	INPUT
M14	1	I/O	←→	I/O	←	INPUT	→	I/O
N2	3	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)	→	VREF(I/O)
N7	2	N.C.	→	I/O	←→	I/O	←	N.C.
N14	1	N.C.	→	I/O	←→	I/O	←	N.C.
N15	1	N.C.	→	VREF	←→	VREF	←	N.C.
P7	2	N.C.	→	I/O	←→	I/O	←	N.C.
P10	2	N.C.	→	I/O	←→	I/O	←	N.C.
R10	2	N.C.	→	VREF	←→	VREF	←	N.C.
T12	2	INPUT	←→	INPUT	→	I/O	←	INPUT
DIFFERENCES			**19**		**7**		**26**	

Legend:

←→	This pin is identical on the device on the left and the right.
→	This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.
←	This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

FT256 Footprint



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	TDI	INPUT	I/O L17N_0 VREF_0	I/O L17P_0	VCCAUX	I/O	INPUT L10P_0 GCLK8	I/O L09N_0 GCLK7	I/O L09P_0 GCLK6	VCCAUX	I/O	I/O L03N_0 VREF_0	I/O L01N_0	TCK	GND
B	I/O L01P_3	I/O L01N_3	I/O L19N_0 HSWAP	I/O	VCCO_0	INPUT ←→	I/O L13P_0 ◆	INPUT L10N_0 GCLK9	GND	INPUT ←→	I/O L05N_0 VREF_0	VCCO_0	I/O L03P_0	I/O L01P_0	TMS	INPUT
C	I/O L02P_3	I/O L02N_3 VREF_3	I/O L19P_0	I/O L18N_0	I/O L18P_0	I/O L15P_0	I/O L13N_0 ◆	I/O L11P_0 GCLK10	INPUT L07N_0	INPUT L07P_0	I/O L05P_0	INPUT L02N_0	INPUT	TDO	I/O L19N_1 LDC2	I/O L19P_1 LDC1
D	I/O L05P_3	INPUT	PROG_B	VCCINT	INPUT L16P_0	I/O L15N_0	I/O L14N_0 VREF_0	I/O L11N_0 GCLK11	I/O VREF_0	I/O L06P_0	I/O L04P_0	INPUT L02P_0	VCCINT	I/O L18N_1 LDC0	I/O L18P_1 HDC	INPUT VREF_1 ←→
E	I/O L05N_3	VCCO_3	I/O L03P_3	I/O L03N_3	VCCINT	INPUT L16N_0	I/O L14P_0	I/O L12P_0	I/O L08P_0 GCLK4	I/O L06N_0	I/O L04N_0	VCCINT	I/O L17P_1 ◆	INPUT	VCCO_1	I/O L17N_1 ◆
F	VCCAUX	INPUT	I/O L04P_3 ◆	I/O L04N_3 VREF_3 ◆	INPUT ←→	GND	VCCO_0	I/O L12N_0	I/O L08N_0 GCLK5	VCCO_0	GND	I/O L16N_1	I/O L16P_1	I/O L15P_1	I/O L15N_1	VCCAUX
G	INPUT VREF_3	I/O L07N_3	I/O L07P_3	I/O L06N_3	I/O L06P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	I/O L14P_1	I/O L14N_1 A0	I/O L13P_1 A2	I/O L13N_1 A1
H	INPUT	GND	I/O L09P_3 LHCLK2	I/O L09N_3 LHCLK3 IRDY2	I/O L08P_3 LHCLK0	I/O L08N_3 LHCLK1	GND	GND	GND	GND	I/O L12N_1 A3 RHCLK7	I/O L12P_1 A4 RHCLK6	INPUT VREF_1	I/O L11N_1 A5 RHCLK5	I/O L11P_1 A6 RHCLK4 IRDY1	INPUT
J	I/O L12P_3	I/O L10P_3 LHCLK4 TRDY2	I/O L10N_3 LHCLK5	I/O L11N_3 LHCLK7	I/O L11P_3 LHCLK6	INPUT	GND	GND	GND	GND	INPUT	INPUT	I/O L10N_1 A7 RHCLK3 TRDY1	I/O L10P_1 A8 RHCLK2	GND	I/O L09N_1 A9 RHCLK1
K	I/O L12N_3	I/O L13P_3	I/O L13N_3	INPUT	I/O L15P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	I/O L07N_1 A11	I/O L07P_1 A12	I/O L08N_1 VREF_1	I/O L08P_1	I/O L09P_1 A10 RHCLK0
L	VCCAUX	I/O L14N_3 VREF_3 ◆	I/O L14P_3 ◆	I/O L17N_3 ◆	I/O L15N_3	GND	VCCO_2	I/O L09N_2 D6 GCLK13	I/O L13P_2 M0	VCCO_2	GND	I/O L05P_1 ◆	I/O L05N_1 ◆	I/O L06P_1	I/O L06N_1	VCCAUX
M	I/O L16P_3	VCCO_3	INPUT	I/O L17P_3 ◆	VCCINT	I/O L05P_2	INPUT ←→	I/O L09P_2 D7 GCLK12	I/O L13N_2 DIN D0	I/O L15N_2	INPUT L17N_2	VCCINT	INPUT	INPUT ←→	VCCO_1	I/O L04N_1 VREF_1
N	I/O L16N_3	INPUT VREF_3 ←→	INPUT	VCCINT	I/O L03N_2 MOSI CSI_B	I/O L05N_2	I/O L07P_2 ◆	I/O L10P_2 D4 GCLK14	I/O L12N_2 D1 GCLK3	I/O L15P_2	INPUT L17P_2	I/O L18N_2 A20	VCCINT	I/O L03P_1 ◆	I/O L03N_1 VREF_1 ◆	I/O L04P_1
P	I/O L18N_3	I/O L18P_3	I/O L01P_2 CSO_B	I/O L01N_2 INIT_B	I/O L03P_2 DOUT BUSY	I/O L06N_2	I/O L07N_2 ◆	I/O L10N_2 D3 GCLK15	I/O L12P_2 D2 GCLK2	I/O L14P_2 ◆	I/O L16N_2 A22	I/O L18P_2 A21	I/O VREF_2	I/O L20P_2 VS0 A17	I/O L02N_1 A13	I/O L02P_1 A14
R	I/O L19N_3	I/O L19P_3	INPUT L02N_2	I/O VREF_2	VCCO_2	I/O L06P_2	INPUT L08P_2	GND	INPUT L11N_2 M2 GCLK1	I/O L14N_2 VREF_2 ◆	I/O L16P_2 A23	VCCO_2	I/O L19N_2 VS1 A18	I/O L20N_2 CCLK	I/O L01N_1 A15	I/O L01P_1 A16
T	GND	INPUT	INPUT L02P_2	I/O L04P_2	I/O L04N_2	VCCAUX	INPUT L08N_2 VREF_2	I/O D5	INPUT L11P_2 RDWR_B GCLK0	I/O M1	VCCAUX	INPUT ←→	I/O L19P_2 VS2 A19	INPUT	DONE	GND

Figure 87: **FT256 Package Footprint (top view)**

2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	8	**VCCINT:** Internal core supply voltage (+1.2V)
28	**GND:** Ground	16	**VCCO:** Output voltage supply for bank	8	**VCCAUX:** Auxiliary supply voltage (+2.5V)
6 ←→	**Migration Difference:** For flexible package migration, use these pins as inputs.	18 (◆)	Unconnected pins on XC3S250E		

FG320: 320-ball Fine-pitch Ball Grid Array

The 320-ball fine-pitch ball grid array package, FG320, supports three different Spartan-3E FPGAs, including the XC3S500E, the XC3S1200E, and the XC3S1600E, as shown in Table 145 and Figure 88.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

Table 145 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs. The XC3S500E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 145 and with the black diamond character (◆) in Table 145 and Figure 88.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S500E FPGA maps to a VREF pin on the XC3S1200E and XC3S1600E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S500E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 144 summarizes the Spartan-3E footprint migration differences for the FG320 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at http://www.xilinx.com/bvdocs/publications/s3e_pin.zip.

Pinout Table

Table 145: **FG320 Package Pinout**

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	IP	IO	IO	A7	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	A8	I/O
0	IO	IO	IO	A11	I/O
0	N.C. (◆)	IO	IO	A12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	C4	I/O
0	IP	IO	IO	D13	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	E13	I/O
0	IO	IO	IO	G9	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B11	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A16	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B16	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	C14	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	D14	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	A14	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	B14	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B13	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	A13	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E12	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	F12	I/O

Table 145: **FG320 Package Pinout *(Continued)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	F11	I/O
0	IO_L08P_0	IO_L08P_0	IO_L08P_0	E11	I/O
0	IO_L09N_0	IO_L09N_0	IO_L09N_0	D11	I/O
0	IO_L09P_0	IO_L09P_0	IO_L09P_0	C11	I/O
0	IO_L11N_0/GCLK5	IO_L11N_0/GCLK5	IO_L11N_0/GCLK5	E10	GCLK
0	IO_L11P_0/GCLK4	IO_L11P_0/GCLK4	IO_L11P_0/GCLK4	D10	GCLK
0	IO_L12N_0/GCLK7	IO_L12N_0/GCLK7	IO_L12N_0/GCLK7	A10	GCLK
0	IO_L12P_0/GCLK6	IO_L12P_0/GCLK6	IO_L12P_0/GCLK6	B10	GCLK
0	IO_L14N_0/GCLK11	IO_L14N_0/GCLK11	IO_L14N_0/GCLK11	D9	GCLK
0	IO_L14P_0/GCLK10	IO_L14P_0/GCLK10	IO_L14P_0/GCLK10	C9	GCLK
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	F9	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	E9	I/O
0	IO_L17N_0	IO_L17N_0	IO_L17N_0	F8	I/O
0	IO_L17P_0	IO_L17P_0	IO_L17P_0	E8	I/O
0	IO_L18N_0/VREF_0	IO_L18N_0/VREF_0	IO_L18N_0/VREF_0	D7	VREF
0	IO_L18P_0	IO_L18P_0	IO_L18P_0	C7	I/O
0	IO_L19N_0/VREF_0	IO_L19N_0/VREF_0	IO_L19N_0/VREF_0	E7	VREF
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	F7	I/O
0	IO_L20N_0	IO_L20N_0	IO_L20N_0	A6	I/O
0	IO_L20P_0	IO_L20P_0	IO_L20P_0	B6	I/O
0	N.C. (◆)	IO_L21N_0	IO_L21N_0	E6	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	N.C. (◆)	IO_L21P_0	IO_L21P_0	D6	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	IO_L23N_0/VREF_0	IO_L23N_0/VREF_0	IO_L23N_0/VREF_0	D5	VREF
0	IO_L23P_0	IO_L23P_0	IO_L23P_0	C5	I/O
0	IO_L24N_0	IO_L24N_0	IO_L24N_0	B4	I/O
0	IO_L24P_0	IO_L24P_0	IO_L24P_0	A4	I/O
0	IO_L25N_0/HSWAP	IO_L25N_0/HSWAP	IO_L25N_0/HSWAP	B3	DUAL
0	IO_L25P_0	IO_L25P_0	IO_L25P_0	C3	I/O
0	IP	IP	IP	A3	INPUT
0	IP	IP	IP	C15	INPUT
0	IP_L02N_0	IP_L02N_0	IP_L02N_0	A15	INPUT
0	IP_L02P_0	IP_L02P_0	IP_L02P_0	B15	INPUT
0	IP_L07N_0	IP_L07N_0	IP_L07N_0	D12	INPUT
0	IP_L07P_0	IP_L07P_0	IP_L07P_0	C12	INPUT
0	IP_L10N_0	IP_L10N_0	IP_L10N_0	G10	INPUT
0	IP_L10P_0	IP_L10P_0	IP_L10P_0	F10	INPUT
0	IP_L13N_0/GCLK9	IP_L13N_0/GCLK9	IP_L13N_0/GCLK9	B9	GCLK

Table 145: **FG320 Package Pinout *(Continued)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	IP_L13P_0/GCLK8	IP_L13P_0/GCLK8	IP_L13P_0/GCLK8	B8	GCLK
0	IP_L16N_0	IP_L16N_0	IP_L16N_0	D8	INPUT
0	IP_L16P_0	IP_L16P_0	IP_L16P_0	C8	INPUT
0	IP_L22N_0	IP_L22N_0	IP_L22N_0	B5	INPUT
0	IP_L22P_0	IP_L22P_0	IP_L22P_0	A5	INPUT
0	VCCO_0	VCCO_0	VCCO_0	A9	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C6	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G11	VCCO
1	N.C. (◆)	IO	IO	P16	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L01N_1/A15	IO_L01N_1/A15	IO_L01N_1/A15	T17	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	IO_L01P_1/A16	U18	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	IO_L02N_1/A13	T18	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	IO_L02P_1/A14	R18	DUAL
1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	R16	VREF
1	IO_L03P_1	IO_L03P_1	IO_L03P_1	R15	I/O
1	N.C. (◆)	IO_L04N_1	IO_L04N_1	N14	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	N.C. (◆)	IO_L04P_1	IO_L04P_1	N15	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	M13	VREF
1	IO_L05P_1	IO_L05P_1	IO_L05P_1	M14	I/O
1	IO_L06N_1	IO_L06N_1	IO_L06N_1	P18	I/O
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	P17	I/O
1	IO_L07N_1	IO_L07N_1	IO_L07N_1	M16	I/O
1	IO_L07P_1	IO_L07P_1	IO_L07P_1	M15	I/O
1	IO_L08N_1	IO_L08N_1	IO_L08N_1	M18	I/O
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	N18	I/O
1	IO_L09N_1/A11	IO_L09N_1/A11	IO_L09N_1/A11	L15	DUAL
1	IO_L09P_1/A12	IO_L09P_1/A12	IO_L09P_1/A12	L16	DUAL
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	L17	VREF
1	IO_L10P_1	IO_L10P_1	IO_L10P_1	L18	I/O
1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	K12	RHCLK/DUAL
1	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	K13	RHCLK/DUAL
1	IO_L12N_1/A7/RHCLK3/TRDY1	IO_L12N_1/A7/RHCLK3/TRDY1	IO_L12N_1/A7/RHCLK3/TRDY1	K14	RHCLK/DUAL
1	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	K15	RHCLK/DUAL

Table 145: **FG320 Package Pinout *(Continued)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
1	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	J16	RHCLK/DUAL
1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	J17	RHCLK/DUAL
1	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	J14	RHCLK/DUAL
1	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	J15	RHCLK/DUAL
1	IO_L15N_1/A1	IO_L15N_1/A1	IO_L15N_1/A1	J13	DUAL
1	IO_L15P_1/A2	IO_L15P_1/A2	IO_L15P_1/A2	J12	DUAL
1	IO_L16N_1/A0	IO_L16N_1/A0	IO_L16N_1/A0	H17	DUAL
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	H16	I/O
1	IO_L17N_1	IO_L17N_1	IO_L17N_1	H15	I/O
1	IO_L17P_1	IO_L17P_1	IO_L17P_1	H14	I/O
1	IO_L18N_1	IO_L18N_1	IO_L18N_1	G16	I/O
1	IO_L18P_1	IO_L18P_1	IO_L18P_1	G15	I/O
1	IO_L19N_1	IO_L19N_1	IO_L19N_1	F17	I/O
1	IO_L19P_1	IO_L19P_1	IO_L19P_1	F18	I/O
1	IO_L20N_1	IO_L20N_1	IO_L20N_1	G13	I/O
1	IO_L20P_1	IO_L20P_1	IO_L20P_1	G14	I/O
1	IO_L21N_1	IO_L21N_1	IO_L21N_1	F14	I/O
1	IO_L21P_1	IO_L21P_1	IO_L21P_1	F15	I/O
1	N.C. (◆)	IO_L22N_1	IO_L22N_1	E16	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	N.C. (◆)	IO_L22P_1	IO_L22P_1	E15	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L23N_1/LDC0	IO_L23N_1/LDC0	IO_L23N_1/LDC0	D16	DUAL
1	IO_L23P_1/HDC	IO_L23P_1/HDC	IO_L23P_1/HDC	D17	DUAL
1	IO_L24N_1/LDC2	IO_L24N_1/LDC2	IO_L24N_1/LDC2	C17	DUAL
1	IO_L24P_1/LDC1	IO_L24P_1/LDC1	IO_L24P_1/LDC1	C18	DUAL
1	IP	IP	IP	B18	INPUT
1	IO	IP	IP	E17	**500E:** I/O **1200E:** INPUT **1600E:** INPUT
1	IP	IP	IP	E18	INPUT
1	IP	IP	IP	G18	INPUT
1	IP	IP	IP	H13	INPUT
1	IP	IP	IP	K17	INPUT
1	IP	IP	IP	K18	INPUT
1	IP	IP	IP	L13	INPUT
1	IP	IP	IP	L14	INPUT
1	IP	IP	IP	N17	INPUT

Table 145: **FG320 Package Pinout *(Continued)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
1	IO	IP	IP	P15	**500E:** I/O **1200E:** INPUT **1600E:** INPUT
1	IP	IP	IP	R17	INPUT
1	IP/VREF_1	IP/VREF_1	IP/VREF_1	D18	VREF
1	IP/VREF_1	IP/VREF_1	IP/VREF_1	H18	VREF
1	VCCO_1	VCCO_1	VCCO_1	F16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	H12	VCCO
1	VCCO_1	VCCO_1	VCCO_1	J18	VCCO
1	VCCO_1	VCCO_1	VCCO_1	L12	VCCO
1	VCCO_1	VCCO_1	VCCO_1	N16	VCCO
2	IO	IO	IO	P9	I/O
2	IO	IO	IO	R11	I/O
2	IP	IO	IO	U6	**500E:** INPUT **1200E:** I/O **1600E:** I/O
2	IP	IO	IO	U13	**500E:** INPUT **1200E:** I/O **1600E:** I/O
2	N.C. (◆)	IO	IO	V7	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO/D5	IO/D5	IO/D5	R9	DUAL
2	IO/M1	IO/M1	IO/M1	V11	DUAL
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	T15	VREF
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	U5	VREF
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	T3	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	U3	DUAL
2	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	T4	DUAL
2	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	U4	DUAL
2	IO_L04N_2	IO_L04N_2	IO_L04N_2	T5	I/O
2	IO_L04P_2	IO_L04P_2	IO_L04P_2	R5	I/O
2	IO_L05N_2	IO_L05N_2	IO_L05N_2	P6	I/O
2	IO_L05P_2	IO_L05P_2	IO_L05P_2	R6	I/O
2	N.C. (◆)	IO_L06N_2/VREF_2	IO_L06N_2/VREF_2	V6	**500E:** N.C. **1200E:** VREF **1600E:** VREF
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	V5	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO_L07N_2	IO_L07N_2	IO_L07N_2	P7	I/O
2	IO_L07P_2	IO_L07P_2	IO_L07P_2	N7	I/O

Table 145: **FG320 Package Pinout *(Continued)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
2	IO_L09N_2	IO_L09N_2	IO_L09N_2	N8	I/O
2	IO_L09P_2	IO_L09P_2	IO_L09P_2	P8	I/O
2	IO_L10N_2	IO_L10N_2	IO_L10N_2	T8	I/O
2	IO_L10P_2	IO_L10P_2	IO_L10P_2	R8	I/O
2	IO_L12N_2/D6/GCLK13	IO_L12N_2/D6/GCLK13	IO_L12N_2/D6/GCLK13	M9	DUAL/GCLK
2	IO_L12P_2/D7/GCLK12	IO_L12P_2/D7/GCLK12	IO_L12P_2/D7/GCLK12	N9	DUAL/GCLK
2	IO_L13N_2/D3/GCLK15	IO_L13N_2/D3/GCLK15	IO_L13N_2/D3/GCLK15	V9	DUAL/GCLK
2	IO_L13P_2/D4/GCLK14	IO_L13P_2/D4/GCLK14	IO_L13P_2/D4/GCLK14	U9	DUAL/GCLK
2	IO_L15N_2/D1/GCLK3	IO_L15N_2/D1/GCLK3	IO_L15N_2/D1/GCLK3	P10	DUAL/GCLK
2	IO_L15P_2/D2/GCLK2	IO_L15P_2/D2/GCLK2	IO_L15P_2/D2/GCLK2	R10	DUAL/GCLK
2	IO_L16N_2/DIN/D0	IO_L16N_2/DIN/D0	IO_L16N_2/DIN/D0	N10	DUAL
2	IO_L16P_2/M0	IO_L16P_2/M0	IO_L16P_2/M0	M10	DUAL
2	IO_L18N_2	IO_L18N_2	IO_L18N_2	N11	I/O
2	IO_L18P_2	IO_L18P_2	IO_L18P_2	P11	I/O
2	IO_L19N_2/VREF_2	IO_L19N_2/VREF_2	IO_L19N_2/VREF_2	V13	VREF
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	V12	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	R12	I/O
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	T12	I/O
2	N.C. (◆)	IO_L21N_2	IO_L21N_2	P12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	N.C. (◆)	IO_L21P_2	IO_L21P_2	N12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO_L22N_2/A22	IO_L22N_2/A22	IO_L22N_2/A22	R13	DUAL
2	IO_L22P_2/A23	IO_L22P_2/A23	IO_L22P_2/A23	P13	DUAL
2	IO_L24N_2/A20	IO_L24N_2/A20	IO_L24N_2/A20	R14	DUAL
2	IO_L24P_2/A21	IO_L24P_2/A21	IO_L24P_2/A21	T14	DUAL
2	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	U15	DUAL
2	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	V15	DUAL
2	IO_L26N_2/CCLK	IO_L26N_2/CCLK	IO_L26N_2/CCLK	U16	DUAL
2	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	T16	DUAL
2	IP	IP	IP	V2	INPUT
2	IP	IP	IP	V16	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	V3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	V4	INPUT
2	IP_L08N_2	IP_L08N_2	IP_L08N_2	R7	INPUT
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	T7	INPUT
2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	V8	VREF
2	IP_L11P_2	IP_L11P_2	IP_L11P_2	U8	INPUT
2	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	T10	DUAL/GCLK

Table 145: **FG320 Package Pinout *(Continued)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
2	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	U10	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	U11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	T11	INPUT
2	IP_L23N_2	IP_L23N_2	IP_L23N_2	U14	INPUT
2	IP_L23P_2	IP_L23P_2	IP_L23P_2	V14	INPUT
2	VCCO_2	VCCO_2	VCCO_2	M8	VCCO
2	VCCO_2	VCCO_2	VCCO_2	M11	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T6	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T13	VCCO
2	VCCO_2	VCCO_2	VCCO_2	V10	VCCO
3	N.C. (◆)	IO	IO	D4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	C2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	C1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	D1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E2	I/O
3	N.C. (◆)	IO_L04N_3	IO_L04N_3	E3	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	N.C. (◆)	IO_L04P_3	IO_L04P_3	E4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L05N_3	IO_L05N_3	IO_L05N_3	F2	I/O
3	IO_L05P_3	IO_L05P_3	IO_L05P_3	F1	I/O
3	IO_L06N_3/VREF_3	IO_L06N_3/VREF_3	IO_L06N_3/VREF_3	G4	VREF
3	IO_L06P_3	IO_L06P_3	IO_L06P_3	G3	I/O
3	IO_L07N_3	IO_L07N_3	IO_L07N_3	G5	I/O
3	IO_L07P_3	IO_L07P_3	IO_L07P_3	G6	I/O
3	IO_L08N_3	IO_L08N_3	IO_L08N_3	H5	I/O
3	IO_L08P_3	IO_L08P_3	IO_L08P_3	H6	I/O
3	IO_L09N_3	IO_L09N_3	IO_L09N_3	H3	I/O
3	IO_L09P_3	IO_L09P_3	IO_L09P_3	H4	I/O
3	IO_L10N_3	IO_L10N_3	IO_L10N_3	H1	I/O
3	IO_L10P_3	IO_L10P_3	IO_L10P_3	H2	I/O
3	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	J4	LHCLK
3	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	J5	LHCLK
3	IO_L12N_3/LHCLK3/ IRDY2	IO_L12N_3/LHCLK3/ IRDY2	IO_L12N_3/LHCLK3/ IRDY2	J2	LHCLK

Table 145: **FG320 Package Pinout *(Continued)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
3	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	J1	LHCLK
3	IO_L13N_3/LHCLK5	IO_L13N_3/LHCLK5	IO_L13N_3/LHCLK5	K4	LHCLK
3	IO_L13P_3/LHCLK4/ TRDY2	IO_L13P_3/LHCLK4/ TRDY2	IO_L13P_3/LHCLK4/ TRDY2	K3	LHCLK
3	IO_L14N_3/LHCLK7	IO_L14N_3/LHCLK7	IO_L14N_3/LHCLK7	K5	LHCLK
3	IO_L14P_3/LHCLK6	IO_L14P_3/LHCLK6	IO_L14P_3/LHCLK6	K6	LHCLK
3	IO_L15N_3	IO_L15N_3	IO_L15N_3	L2	I/O
3	IO_L15P_3	IO_L15P_3	IO_L15P_3	L1	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	L4	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	L3	I/O
3	IO_L17N_3/VREF_3	IO_L17N_3/VREF_3	IO_L17N_3/VREF_3	L5	VREF
3	IO_L17P_3	IO_L17P_3	IO_L17P_3	L6	I/O
3	IO_L18N_3	IO_L18N_3	IO_L18N_3	M3	I/O
3	IO_L18P_3	IO_L18P_3	IO_L18P_3	M4	I/O
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	M6	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	M5	I/O
3	IO_L20N_3	IO_L20N_3	IO_L20N_3	N5	I/O
3	IO_L20P_3	IO_L20P_3	IO_L20P_3	N4	I/O
3	IO_L21N_3	IO_L21N_3	IO_L21N_3	P1	I/O
3	IO_L21P_3	IO_L21P_3	IO_L21P_3	P2	I/O
3	N.C. (◆)	IO_L22N_3	IO_L22N_3	P4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	N.C. (◆)	IO_L22P_3	IO_L22P_3	P3	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L23N_3	IO_L23N_3	IO_L23N_3	R2	I/O
3	IO_L23P_3	IO_L23P_3	IO_L23P_3	R3	I/O
3	IO_L24N_3	IO_L24N_3	IO_L24N_3	T1	I/O
3	IO_L24P_3	IO_L24P_3	IO_L24P_3	T2	I/O
3	IP	IP	IP	D3	INPUT
3	IO	IP	IP	F4	**500E:** I/O **1200E:** INPUT **1600E:** INPUT
3	IP	IP	IP	F5	INPUT
3	IP	IP	IP	G1	INPUT
3	IP	IP	IP	J7	INPUT
3	IP	IP	IP	K2	INPUT
3	IP	IP	IP	K7	INPUT
3	IP	IP	IP	M1	INPUT
3	IP	IP	IP	N1	INPUT
3	IP	IP	IP	N2	INPUT

Table 145: **FG320 Package Pinout *(Continued)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
3	IP	IP	IP	R1	INPUT
3	IP	IP	IP	U1	INPUT
3	IP/VREF_3	IP/VREF_3	IP/VREF_3	J6	VREF
3	IO/VREF_3	IP/VREF_3	IP/VREF_3	R4	**500E:** VREF(I/O) **1200E:** VREF(INPUT) **1600E:** VREF(INPUT)
3	VCCO_3	VCCO_3	VCCO_3	F3	VCCO
3	VCCO_3	VCCO_3	VCCO_3	H7	VCCO
3	VCCO_3	VCCO_3	VCCO_3	K1	VCCO
3	VCCO_3	VCCO_3	VCCO_3	L7	VCCO
3	VCCO_3	VCCO_3	VCCO_3	N3	VCCO
GND	GND	GND	GND	A1	GND
GND	GND	GND	GND	A18	GND
GND	GND	GND	GND	B2	GND
GND	GND	GND	GND	B17	GND
GND	GND	GND	GND	C10	GND
GND	GND	GND	GND	G7	GND
GND	GND	GND	GND	G12	GND
GND	GND	GND	GND	H8	GND
GND	GND	GND	GND	H9	GND
GND	GND	GND	GND	H10	GND
GND	GND	GND	GND	H11	GND
GND	GND	GND	GND	J3	GND
GND	GND	GND	GND	J8	GND
GND	GND	GND	GND	J11	GND
GND	GND	GND	GND	K8	GND
GND	GND	GND	GND	K11	GND
GND	GND	GND	GND	K16	GND
GND	GND	GND	GND	L8	GND
GND	GND	GND	GND	L9	GND
GND	GND	GND	GND	L10	GND
GND	GND	GND	GND	L11	GND
GND	GND	GND	GND	M7	GND
GND	GND	GND	GND	M12	GND
GND	GND	GND	GND	T9	GND
GND	GND	GND	GND	U2	GND
GND	GND	GND	GND	U17	GND
GND	GND	GND	GND	V1	GND
GND	GND	GND	GND	V18	GND
VCCAUX	DONE	DONE	DONE	V17	CONFIG

Table 145: **FG320 Package Pinout *(Continued)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
VCCAUX	PROG_B	PROG_B	PROG_B	B1	CONFIG
VCCAUX	TCK	TCK	TCK	A17	JTAG
VCCAUX	TDI	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	TDO	C16	JTAG
VCCAUX	TMS	TMS	TMS	D15	JTAG
VCCAUX	VCCAUX	VCCAUX	VCCAUX	B7	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	B12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	G2	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	G17	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	M2	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	M17	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	U7	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	U12	VCCAUX
VCCINT	VCCINT	VCCINT	VCCINT	E5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	E14	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	F6	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	F13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N6	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	P5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	P14	VCCINT

User I/Os by Bank

Table 146 and Table 147 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package.

Table 146: **User I/Os Per Bank for XC3S500E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	58	29	14	1	6	8
Right	1	58	22	10	21	5	0[1]
Bottom	2	58	17	13	24	4	0[1]
Left	3	58	34	11	0	5	8
TOTAL		**232**	**102**	**48**	**46**	**20**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 147: **User I/Os Per Bank for XC3S1200E and XC3S1600E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	61	34	12	1	6	8
Right	1	63	25	12	21	5	0[1]
Bottom	2	63	23	11	24	5	0[1]
Left	3	63	38	12	0	5	8
TOTAL		**250**	**120**	**47**	**46**	**21**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

Table 148 summarizes any footprint and functionality differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs that may affect easy migration between devices available in the FG320 package. There are 26 such balls. All other pins not listed in Table 148 unconditionally migrate between Spartan-3E devices available in the FG320 package.

The XC3S500E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S1200E and the XC3S1600E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 148: **FG320 Footprint Migration Differences**

Pin	Bank	XC3S500E	Migration	XC3S1200E	Migration	XC3S1600E	Migration	XC3S500E
A7	0	INPUT	→	I/O	←→	I/O	←	INPUT
A12	0	N.C.	→	I/O	←→	I/O	←	N.C.
D4	3	N.C.	→	I/O	←→	I/O	←	N.C.
D6	0	N.C.	→	I/O	←→	I/O	←	N.C.
D13	0	INPUT	→	I/O	←→	I/O	←	INPUT
E3	3	N.C.	→	I/O	←→	I/O	←	N.C.
E4	3	N.C.	→	I/O	←→	I/O	←	N.C.
E6	0	N.C.	→	I/O	←→	I/O	←	N.C.
E15	1	N.C.	→	I/O	←→	I/O	←	N.C.
E16	1	N.C.	→	I/O	←→	I/O	←	N.C.
E17	1	I/O	←	INPUT	←→	INPUT	←	I/O
F4	3	I/O	←	INPUT	←→	INPUT	←	I/O
N12	2	N.C.	→	I/O	←→	I/O	←	N.C.
N14	1	N.C.	→	I/O	←→	I/O	←	N.C.
N15	1	N.C.	→	I/O	←→	I/O	←	N.C.
P3	3	N.C.	→	I/O	←→	I/O	←	N.C.
P4	3	N.C.	→	I/O	←→	I/O	←	N.C.
P12	2	N.C.	→	I/O	←→	I/O	←	N.C.
P15	1	I/O	←	INPUT	←→	INPUT	→	I/O
P16	1	N.C.	→	I/O	←→	I/O	←	N.C.
R4	3	VREF(I/O)	←	VREF(INPUT)	←→	VREF(INPUT)	→	VREF(I/O)
U6	2	INPUT	→	I/O	←→	I/O	←	INPUT
U13	2	INPUT	→	I/O	←→	I/O	←	INPUT
V5	2	N.C.	→	I/O	←→	I/O	←	N.C.
V6	2	N.C.	→	VREF	←→	VREF	←	N.C.
V7	2	N.C.	→	I/O	←→	I/O	←	N.C.
DIFFERENCES			**26**		**0**		**26**	

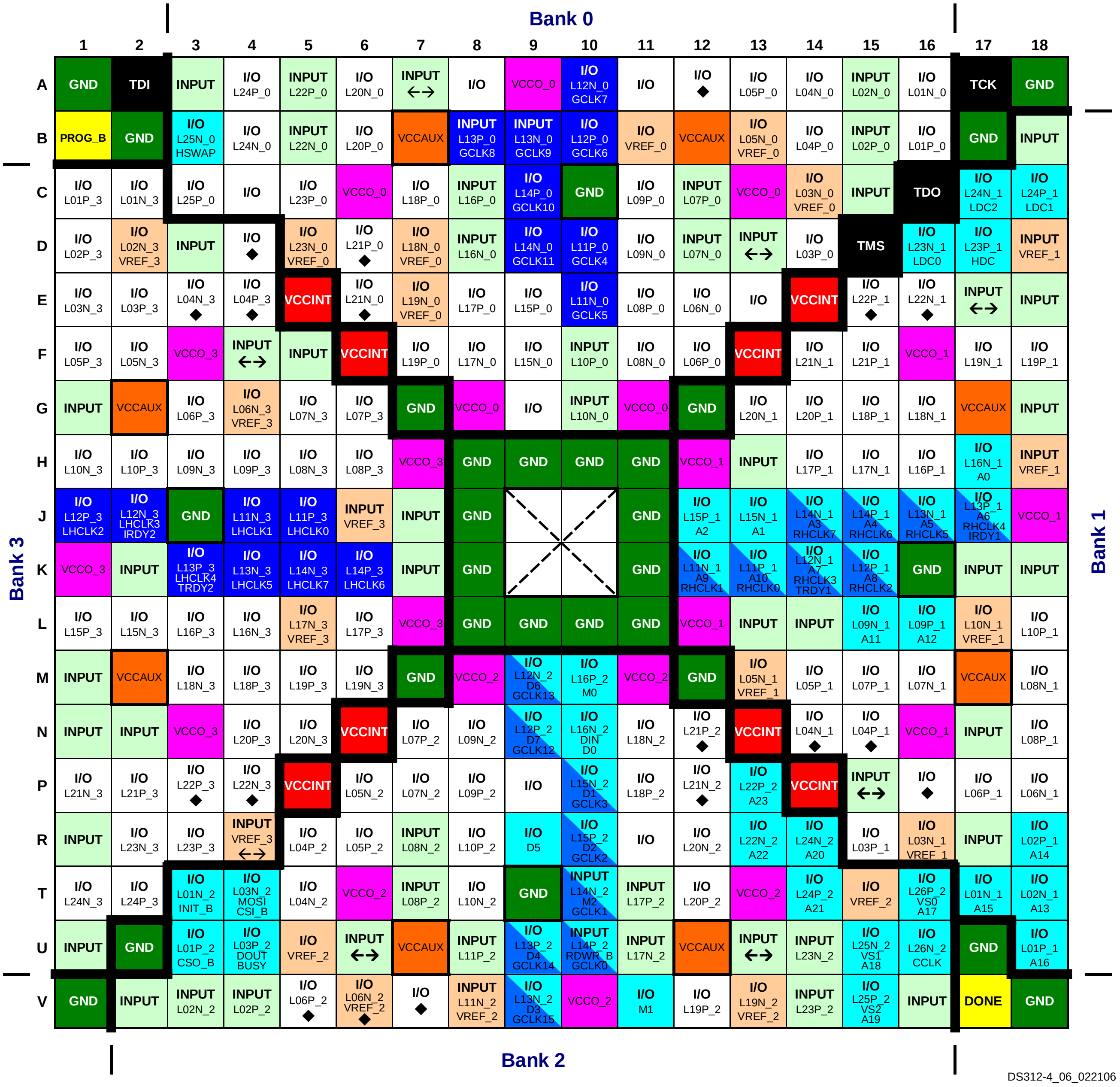
Legend:

←→ This pin is identical on the device on the left and the right.

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

FG320 Footprint



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	TDI	INPUT	I/O L24P_0	INPUT L22P_0	I/O L20N_0	INPUT ←→	I/O	VCCO_0	I/O L12N_0 GCLK7	I/O	I/O ◆	I/O L05P_0	I/O L04N_0	INPUT L02N_0	I/O L01N_0	TCK	GND
B	PROG_B	GND	I/O L25N_0 HSWAP	I/O L24N_0	INPUT L22N_0	I/O L20P_0	VCCAUX	INPUT L13P_0 GCLK8	INPUT L13N_0 GCLK9	I/O L12P_0 GCLK6	I/O VREF_0	VCCAUX	I/O L05N_0 VREF_0	I/O L04P_0	INPUT L02P_0	I/O L01P_0	GND	INPUT
C	I/O L01P_3	I/O L01N_3	I/O L25P_0	I/O	I/O L23P_0	VCCO_0	I/O L18P_0	INPUT L16P_0	I/O L14P_0 GCLK10	GND	I/O L09P_0	INPUT L07P_0	VCCO_0	I/O L03N_0 VREF_0	INPUT	TDO	I/O L24N_1 LDC2	I/O L24P_1 LDC1
D	I/O L02P_3	I/O L02N_3 VREF_3	INPUT	I/O ◆	I/O L23N_0 VREF_0	I/O L21P_0 ◆	I/O L18N_0 VREF_0	INPUT L16N_0	I/O L14N_0 GCLK11	I/O L11P_0 GCLK4	I/O L09N_0	INPUT L07N_0	INPUT ←→	I/O L03P_0	TMS	I/O L23N_1 LDC0	I/O L23P_1 HDC	INPUT VREF_1
E	I/O L03N_3	I/O L03P_3	I/O L04N_3 ◆	I/O L04P_3 ◆	VCCINT	I/O L21N_0 ◆	I/O L19N_0 VREF_0	I/O L17P_0	I/O L15P_0	I/O L11N_0 GCLK5	I/O L08P_0	I/O L06N_0	I/O	VCCINT	I/O L22P_1 ◆	I/O L22N_1 ◆	INPUT ←→	INPUT
F	I/O L05P_3	I/O L05N_3	VCCO_3	INPUT ←→	INPUT	VCCINT	I/O L19P_0	I/O L17N_0	I/O L15N_0	INPUT L10P_0	I/O L08N_0	I/O L06P_0	VCCINT	I/O L21N_1	I/O L21P_1	VCCO_1	I/O L19N_1	I/O L19P_1
G	INPUT	VCCAUX	I/O L06P_3	I/O L06N_3 VREF_3	I/O L07N_3	I/O L07P_3	GND	VCCO_0	I/O	INPUT L10N_0	VCCO_0	GND	I/O L20N_1	I/O L20P_1	I/O L18P_1	I/O L18N_1	VCCAUX	INPUT
H	I/O L10N_3	I/O L10P_3	I/O L09N_3	I/O L09P_3	I/O L08N_3	I/O L08P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	I/O L17P_1	I/O L17N_1	I/O L16P_1	I/O L16N_1 A0	INPUT VREF_1
J	I/O L12P_3 LHCLK2	I/O L12N_3 LHCLK3 IRDY2	GND	I/O L11N_3 LHCLK1	I/O L11P_3 LHCLK0	INPUT VREF_3	INPUT	GND			GND	I/O L15P_1 A2	I/O L15N_1 A1	I/O L14N_1 A3 RHCLK7	I/O L14P_1 A4 RHCLK6	I/O L13N_1 A5 RHCLK5	I/O L13P_1 A6 RHCLK4 IRDY1	VCCO_1
K	VCCO_3	INPUT	I/O L13P_3 LHCLK4 TRDY2	I/O L13N_3 LHCLK5	I/O L14N_3 LHCLK7	I/O L14P_3 LHCLK6	INPUT	GND			GND	I/O L11N_1 A9 RHCLK1	I/O L11P_1 A10 RHCLK0	I/O L12N_1 A7 RHCLK3 TRDY1	I/O L12P_1 A8 RHCLK2	GND	INPUT	INPUT
L	I/O L15P_3	I/O L15N_3	I/O L16P_3	I/O L16N_3	I/O L17N_3 VREF_3	I/O L17P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	INPUT	I/O L09N_1 A11	I/O L09P_1 A12	I/O L10N_1 VREF_1	I/O L10P_1
M	INPUT	VCCAUX	I/O L18N_3	I/O L18P_3	I/O L19P_3	I/O L19N_3	GND	VCCO_2	I/O L12N_2 D6 GCLK13	I/O L16P_2 M0	VCCO_2	GND	I/O L05N_1 VREF_1	I/O L05P_1	I/O L07P_1	I/O L07N_1	VCCAUX	I/O L08N_1
N	INPUT	INPUT	VCCO_3	I/O L20P_3	I/O L20N_3	VCCINT	I/O L07P_2	I/O L09N_2	I/O L12P_2 D7 GCLK12	I/O L16N_2 DIN D0	I/O L18N_2	I/O L21P_2 ◆	VCCINT	I/O L04N_1 ◆	I/O L04P_1 ◆	VCCO_1	INPUT	I/O L08P_1
P	I/O L21N_3	I/O L21P_3	I/O L22P_3 ◆	I/O L22N_3 ◆	VCCINT	I/O L05N_2	I/O L07N_2	I/O L09P_2	I/O	I/O L15N_2 D1 GCLK3	I/O L18P_2	I/O L21N_2 ◆	I/O L22P_2 A23	VCCINT	INPUT ←→	I/O ◆	I/O L06P_1	I/O L06N_1
R	INPUT	I/O L23N_3	I/O L23P_3	INPUT VREF_3 ←→	I/O L04P_2	I/O L05P_2	INPUT L08N_2	I/O L10P_2	I/O D5	I/O L15P_2 D2 GCLK2	I/O	I/O L20N_2	I/O L22N_2 A22	I/O L24N_2 A20	I/O L03P_1	I/O L03N_1 VREF_1	INPUT	I/O L02P_1 A14
T	I/O L24N_3	I/O L24P_3	I/O L01N_2 INIT_B	I/O L03N_2 MOSI CSI_B	I/O L04N_2	VCCO_2	INPUT L08P_2	I/O L10N_2	GND	INPUT L14N_2 M2 GCLK1	INPUT L17P_2	I/O L20P_2	VCCO_2	I/O L24P_2 A21	I/O VREF_2	I/O L26P_2 VS0 A17	I/O L01N_1 A15	I/O L02N_1 A13
U	INPUT	GND	I/O L01P_2 CSO_B	I/O L03P_2 DOUT BUSY	I/O VREF_2	INPUT ←→	VCCAUX	INPUT L11P_2	I/O L13P_2 D4 GCLK14	INPUT L14P_2 RDWR_B GCLK0	INPUT L17N_2	VCCAUX	INPUT ←→	INPUT L23N_2	I/O L25N_2 VS1 A18	I/O L26N_2 CCLK	GND	I/O L01P_1 A16
V	GND	INPUT	INPUT L02N_2	INPUT L02P_2	I/O L06P_2 ◆	I/O L06N_2 VREF_2 ◆	I/O ◆	INPUT L11N_2 VREF_2	I/O L13N_2 D3 GCLK15	VCCO_2	I/O M1	I/O L19P_2	I/O L19N_2 VREF_2	INPUT L23P_2	I/O L25P_2 VS2 A19	INPUT	DONE	GND

Figure 88: **FG320 Package Footprint (top view)**

102-120	**I/O:** Unrestricted, general-purpose user I/O	46	**DUAL:** Configuration pin, then possible user-I/O	20-21	**VREF:** User I/O or input voltage reference for bank
47-48	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	20	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	8	**VCCINT:** Internal core supply voltage (+1.2V)
18	**N.C.:** Not connected. Only the XC3S500E has these pins (◆).	28	**GND:** Ground	8	**VCCAUX:** Auxiliary supply voltage (+2.5V)

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3E FPGAs, including the XC3S1200E and the XC3S1600E. Both devices share a common footprint for this package as shown in Table 149 and Figure 89.

Table 149 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3e_pin.zip.

Pinout Table

Table 149: **FG400 Package Pinout**

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IO	A3	I/O
0	IO	A8	I/O
0	IO	A12	I/O
0	IO	C7	I/O
0	IO	C10	I/O
0	IO	E8	I/O
0	IO	E13	I/O
0	IO	E16	I/O
0	IO	F13	I/O
0	IO	F14	I/O
0	IO	G7	I/O
0	IO/VREF_0	C11	VREF
0	IO_L01N_0	B17	I/O
0	IO_L01P_0	C17	I/O
0	IO_L03N_0/VREF_0	A18	VREF
0	IO_L03P_0	A19	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0	A16	I/O
0	IO_L06N_0	A15	I/O
0	IO_L06P_0	B15	I/O
0	IO_L07N_0	C14	I/O
0	IO_L07P_0	D14	I/O
0	IO_L09N_0/VREF_0	A13	VREF
0	IO_L09P_0	A14	I/O
0	IO_L10N_0	B13	I/O
0	IO_L10P_0	C13	I/O
0	IO_L12N_0	C12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	E12	I/O
0	IO_L13P_0	F12	I/O
0	IO_L15N_0/GCLK5	G11	GCLK
0	IO_L15P_0/GCLK4	F11	GCLK
0	IO_L16N_0/GCLK7	E10	GCLK
0	IO_L16P_0/GCLK6	E11	GCLK
0	IO_L18N_0/GCLK11	A9	GCLK
0	IO_L18P_0/GCLK10	A10	GCLK
0	IO_L19N_0	F9	I/O
0	IO_L19P_0	E9	I/O
0	IO_L21N_0	C9	I/O
0	IO_L21P_0	D9	I/O
0	IO_L22N_0/VREF_0	B8	VREF
0	IO_L22P_0	B9	I/O
0	IO_L24N_0/VREF_0	F7	VREF
0	IO_L24P_0	F8	I/O
0	IO_L25N_0	A6	I/O
0	IO_L25P_0	A7	I/O
0	IO_L27N_0	B5	I/O
0	IO_L27P_0	B6	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C6	I/O
0	IO_L30N_0/VREF_0	C5	VREF
0	IO_L30P_0	D5	I/O
0	IO_L31N_0	A2	I/O
0	IO_L31P_0	B2	I/O
0	IO_L32N_0/HSWAP	D4	DUAL
0	IO_L32P_0	C4	I/O
0	IP	B18	INPUT
0	IP	E5	INPUT
0	IP_L02N_0	C16	INPUT
0	IP_L02P_0	D16	INPUT
0	IP_L05N_0	D15	INPUT
0	IP_L05P_0	C15	INPUT
0	IP_L08N_0	E14	INPUT
0	IP_L08P_0	E15	INPUT
0	IP_L11N_0	G14	INPUT
0	IP_L11P_0	G13	INPUT

Table 149: **FG400 Package Pinout *(Continued)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IP_L14N_0	B11	INPUT
0	IP_L14P_0	B12	INPUT
0	IP_L17N_0/GCLK9	G10	GCLK
0	IP_L17P_0/GCLK8	H10	GCLK
0	IP_L20N_0	G9	INPUT
0	IP_L20P_0	G8	INPUT
0	IP_L23N_0	C8	INPUT
0	IP_L23P_0	D8	INPUT
0	IP_L26N_0	E6	INPUT
0	IP_L26P_0	E7	INPUT
0	IP_L29N_0	A4	INPUT
0	IP_L29P_0	A5	INPUT
0	VCCO_0	B4	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	D7	VCCO
0	VCCO_0	D13	VCCO
0	VCCO_0	F10	VCCO
1	IO_L01N_1/A15	U18	DUAL
1	IO_L01P_1/A16	U17	DUAL
1	IO_L02N_1/A13	T18	DUAL
1	IO_L02P_1/A14	T17	DUAL
1	IO_L03N_1/VREF_1	V19	VREF
1	IO_L03P_1	U19	I/O
1	IO_L04N_1	W20	I/O
1	IO_L04P_1	V20	I/O
1	IO_L05N_1	R18	I/O
1	IO_L05P_1	R17	I/O
1	IO_L06N_1	T20	I/O
1	IO_L06P_1	U20	I/O
1	IO_L07N_1	P18	I/O
1	IO_L07P_1	P17	I/O
1	IO_L08N_1/VREF_1	P20	VREF
1	IO_L08P_1	R20	I/O
1	IO_L09N_1	P16	I/O
1	IO_L09P_1	N16	I/O
1	IO_L10N_1	N19	I/O
1	IO_L10P_1	N18	I/O
1	IO_L11N_1	N15	I/O
1	IO_L11P_1	M15	I/O
1	IO_L12N_1/A11	M18	DUAL
1	IO_L12P_1/A12	M17	DUAL
1	IO_L13N_1/VREF_1	L19	VREF
1	IO_L13P_1	M19	I/O
1	IO_L14N_1/A9/RHCLK1	L16	RHCLK/DUAL
1	IO_L14P_1/A10/RHCLK0	M16	RHCLK/DUAL
1	IO_L15N_1/A7/RHCLK3/TRDY1	L14	RHCLK/DUAL
1	IO_L15P_1/A8/RHCLK2	L15	RHCLK/DUAL
1	IO_L16N_1/A5/RHCLK5	K14	RHCLK/DUAL
1	IO_L16P_1/A6/RHCLK4/IRDY1	K13	RHCLK/DUAL
1	IO_L17N_1/A3/RHCLK7	J20	RHCLK/DUAL
1	IO_L17P_1/A4/RHCLK6	K20	RHCLK/DUAL
1	IO_L18N_1/A1	K16	DUAL
1	IO_L18P_1/A2	J16	DUAL
1	IO_L19N_1/A0	J13	DUAL
1	IO_L19P_1	J14	I/O
1	IO_L20N_1	J17	I/O
1	IO_L20P_1	J18	I/O
1	IO_L21N_1	H19	I/O
1	IO_L21P_1	J19	I/O
1	IO_L22N_1	H15	I/O
1	IO_L22P_1	H16	I/O
1	IO_L23N_1	H18	I/O
1	IO_L23P_1	H17	I/O
1	IO_L24N_1/VREF_1	H20	VREF
1	IO_L24P_1	G20	I/O
1	IO_L25N_1	G16	I/O
1	IO_L25P_1	F16	I/O
1	IO_L26N_1	F19	I/O
1	IO_L26P_1	F20	I/O
1	IO_L27N_1	F18	I/O
1	IO_L27P_1	F17	I/O
1	IO_L28N_1	D20	I/O
1	IO_L28P_1	E20	I/O
1	IO_L29N_1/LDC0	D18	DUAL

Table 149: **FG400 Package Pinout *(Continued)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
1	IO_L29P_1/HDC	E18	DUAL
1	IO_L30N_1/LDC2	C19	DUAL
1	IO_L30P_1/LDC1	C20	DUAL
1	IP	B20	INPUT
1	IP	G15	INPUT
1	IP	G18	INPUT
1	IP	H14	INPUT
1	IP	J15	INPUT
1	IP	L18	INPUT
1	IP	M20	INPUT
1	IP	N14	INPUT
1	IP	N20	INPUT
1	IP	P15	INPUT
1	IP	R16	INPUT
1	IP	R19	INPUT
1	IP/VREF_1	E19	VREF
1	IP/VREF_1	K18	VREF
1	VCCO_1	D19	VCCO
1	VCCO_1	G17	VCCO
1	VCCO_1	K15	VCCO
1	VCCO_1	K19	VCCO
1	VCCO_1	N17	VCCO
1	VCCO_1	T19	VCCO
2	IO	P8	I/O
2	IO	P13	I/O
2	IO	R9	I/O
2	IO	R13	I/O
2	IO	W15	I/O
2	IO	Y5	I/O
2	IO	Y7	I/O
2	IO	Y13	I/O
2	IO/D5	N11	DUAL
2	IO/M1	T11	DUAL
2	IO/VREF_2	Y3	VREF
2	IO/VREF_2	Y17	VREF
2	IO_L01N_2/INIT_B	V4	DUAL
2	IO_L01P_2/CSO_B	U4	DUAL
2	IO_L03N_2/MOSI/CSI_B	V5	DUAL
2	IO_L03P_2/DOUT/BUSY	U5	DUAL
2	IO_L04N_2	Y4	I/O

Table 149: **FG400 Package Pinout *(Continued)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
2	IO_L04P_2	W4	I/O
2	IO_L06N_2	T6	I/O
2	IO_L06P_2	T5	I/O
2	IO_L07N_2	U7	I/O
2	IO_L07P_2	V7	I/O
2	IO_L09N_2/VREF_2	R7	VREF
2	IO_L09P_2	T7	I/O
2	IO_L10N_2	V8	I/O
2	IO_L10P_2	W8	I/O
2	IO_L12N_2	U9	I/O
2	IO_L12P_2	V9	I/O
2	IO_L13N_2	Y8	I/O
2	IO_L13P_2	Y9	I/O
2	IO_L15N_2/D6/GCLK13	W10	DUAL/ GCLK
2	IO_L15P_2/D7/GCLK12	W9	DUAL/ GCLK
2	IO_L16N_2/D3/GCLK15	P10	DUAL/ GCLK
2	IO_L16P_2/D4/GCLK14	R10	DUAL/ GCLK
2	IO_L18N_2/D1/GCLK3	V11	DUAL/ GCLK
2	IO_L18P_2/D2/GCLK2	V10	DUAL/ GCLK
2	IO_L19N_2/DIN/D0	Y12	DUAL
2	IO_L19P_2/M0	Y11	DUAL
2	IO_L21N_2	U12	I/O
2	IO_L21P_2	V12	I/O
2	IO_L22N_2/VREF_2	W12	VREF
2	IO_L22P_2	W13	I/O
2	IO_L24N_2	U13	I/O
2	IO_L24P_2	V13	I/O
2	IO_L25N_2	P14	I/O
2	IO_L25P_2	R14	I/O
2	IO_L27N_2/A22	Y14	DUAL
2	IO_L27P_2/A23	Y15	DUAL
2	IO_L28N_2	T15	I/O
2	IO_L28P_2	U15	I/O
2	IO_L30N_2/A20	V16	DUAL
2	IO_L30P_2/A21	U16	DUAL
2	IO_L31N_2/VS1/A18	Y18	DUAL

Table 149: **FG400 Package Pinout *(Continued)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
2	IO_L31P_2/VS2/A19	W18	DUAL
2	IO_L32N_2/CCLK	W19	DUAL
2	IO_L32P_2/VS0/A17	Y19	DUAL
2	IP	T16	INPUT
2	IP	W3	INPUT
2	IP_L02N_2	Y2	INPUT
2	IP_L02P_2	W2	INPUT
2	IP_L05N_2	V6	INPUT
2	IP_L05P_2	U6	INPUT
2	IP_L08N_2	Y6	INPUT
2	IP_L08P_2	W6	INPUT
2	IP_L11N_2	R8	INPUT
2	IP_L11P_2	T8	INPUT
2	IP_L14N_2/VREF_2	T10	VREF
2	IP_L14P_2	T9	INPUT
2	IP_L17N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L17P_2/RDWR_B/ GCLK0	P11	DUAL/ GCLK
2	IP_L20N_2	T12	INPUT
2	IP_L20P_2	R12	INPUT
2	IP_L23N_2/VREF_2	T13	VREF
2	IP_L23P_2	T14	INPUT
2	IP_L26N_2	V14	INPUT
2	IP_L26P_2	V15	INPUT
2	IP_L29N_2	W16	INPUT
2	IP_L29P_2	Y16	INPUT
2	VCCO_2	R11	VCCO
2	VCCO_2	U8	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	W5	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W17	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	D3	I/O
3	IO_L02N_3/VREF_3	E3	VREF
3	IO_L02P_3	E4	I/O
3	IO_L03N_3	C1	I/O
3	IO_L03P_3	B1	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O

Table 149: **FG400 Package Pinout *(Continued)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IO_L05N_3	F3	I/O
3	IO_L05P_3	F4	I/O
3	IO_L06N_3	F1	I/O
3	IO_L06P_3	F2	I/O
3	IO_L07N_3	G4	I/O
3	IO_L07P_3	G3	I/O
3	IO_L08N_3	G5	I/O
3	IO_L08P_3	H5	I/O
3	IO_L09N_3/VREF_3	H3	VREF
3	IO_L09P_3	H2	I/O
3	IO_L10N_3	H7	I/O
3	IO_L10P_3	H6	I/O
3	IO_L11N_3	J4	I/O
3	IO_L11P_3	J3	I/O
3	IO_L12N_3	J1	I/O
3	IO_L12P_3	J2	I/O
3	IO_L13N_3	J6	I/O
3	IO_L13P_3	K6	I/O
3	IO_L14N_3/LHCLK1	K2	LHCLK
3	IO_L14P_3/LHCLK0	K3	LHCLK
3	IO_L15N_3/LHCLK3/IRDY2	L7	LHCLK
3	IO_L15P_3/LHCLK2	K7	LHCLK
3	IO_L16N_3/LHCLK5	L1	LHCLK
3	IO_L16P_3/LHCLK4/TRDY2	M1	LHCLK
3	IO_L17N_3/LHCLK7	L3	LHCLK
3	IO_L17P_3/LHCLK6	M3	LHCLK
3	IO_L18N_3	M7	I/O
3	IO_L18P_3	M8	I/O
3	IO_L19N_3	M4	I/O
3	IO_L19P_3	M5	I/O
3	IO_L20N_3/VREF_3	N6	VREF
3	IO_L20P_3	M6	I/O
3	IO_L21N_3	N2	I/O
3	IO_L21P_3	N1	I/O
3	IO_L22N_3	P7	I/O
3	IO_L22P_3	N7	I/O
3	IO_L23N_3	N4	I/O
3	IO_L23P_3	N3	I/O
3	IO_L24N_3	R1	I/O
3	IO_L24P_3	P1	I/O

Table 149: **FG400 Package Pinout *(Continued)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IO_L25N_3	R5	I/O
3	IO_L25P_3	P5	I/O
3	IO_L26N_3	T2	I/O
3	IO_L26P_3	R2	I/O
3	IO_L27N_3	R4	I/O
3	IO_L27P_3	R3	I/O
3	IO_L28N_3/VREF_3	T1	VREF
3	IO_L28P_3	U1	I/O
3	IO_L29N_3	T3	I/O
3	IO_L29P_3	U3	I/O
3	IO_L30N_3	V1	I/O
3	IO_L30P_3	V2	I/O
3	IP	F5	INPUT
3	IP	G1	INPUT
3	IP	G6	INPUT
3	IP	H1	INPUT
3	IP	J5	INPUT
3	IP	L5	INPUT
3	IP	L8	INPUT
3	IP	M2	INPUT
3	IP	N5	INPUT
3	IP	P3	INPUT
3	IP	T4	INPUT
3	IP	W1	INPUT
3	IP/VREF_3	K5	VREF
3	IP/VREF_3	P6	VREF
3	VCCO_3	E2	VCCO
3	VCCO_3	H4	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L6	VCCO
3	VCCO_3	P4	VCCO
3	VCCO_3	U2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A20	GND
GND	GND	B7	GND
GND	GND	B14	GND
GND	GND	C3	GND
GND	GND	C18	GND
GND	GND	D10	GND

Table 149: **FG400 Package Pinout *(Continued)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
GND	GND	F6	GND
GND	GND	F15	GND
GND	GND	G2	GND
GND	GND	G12	GND
GND	GND	G19	GND
GND	GND	H8	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	K1	GND
GND	GND	K8	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K17	GND
GND	GND	L4	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L20	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	N13	GND
GND	GND	P2	GND
GND	GND	P9	GND
GND	GND	P19	GND
GND	GND	R6	GND
GND	GND	R15	GND
GND	GND	U11	GND
GND	GND	V3	GND
GND	GND	V18	GND
GND	GND	W7	GND
GND	GND	W14	GND
GND	GND	Y1	GND
GND	GND	Y10	GND
GND	GND	Y20	GND
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C2	CONFIG
VCCAUX	TCK	D17	JTAG
VCCAUX	TDI	B3	JTAG
VCCAUX	TDO	B19	JTAG
VCCAUX	TMS	E17	JTAG

Table 149: **FG400 Package Pinout *(Continued)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
VCCAUX	VCCAUX	D11	VCCAUX
VCCAUX	VCCAUX	H12	VCCAUX
VCCAUX	VCCAUX	J7	VCCAUX
VCCAUX	VCCAUX	K4	VCCAUX
VCCAUX	VCCAUX	L17	VCCAUX
VCCAUX	VCCAUX	M14	VCCAUX
VCCAUX	VCCAUX	N9	VCCAUX
VCCAUX	VCCAUX	U10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	H13	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	N8	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT

User I/Os by Bank

Table 150 indicates how the 304 available user-I/O pins are distributed between the four I/O banks on the FG400 package.

Table 150: **User I/Os Per Bank for the XC3S1200E and XC3S1600E in the FG400 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	78	43	20	1	6	8
Right	1	74	35	12	21	6	0(1)
Bottom	2	78	30	18	24	6	0(1)
Left	3	74	48	12	0	6	8
TOTAL		**304**	**156**	**62**	**46**	**24**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

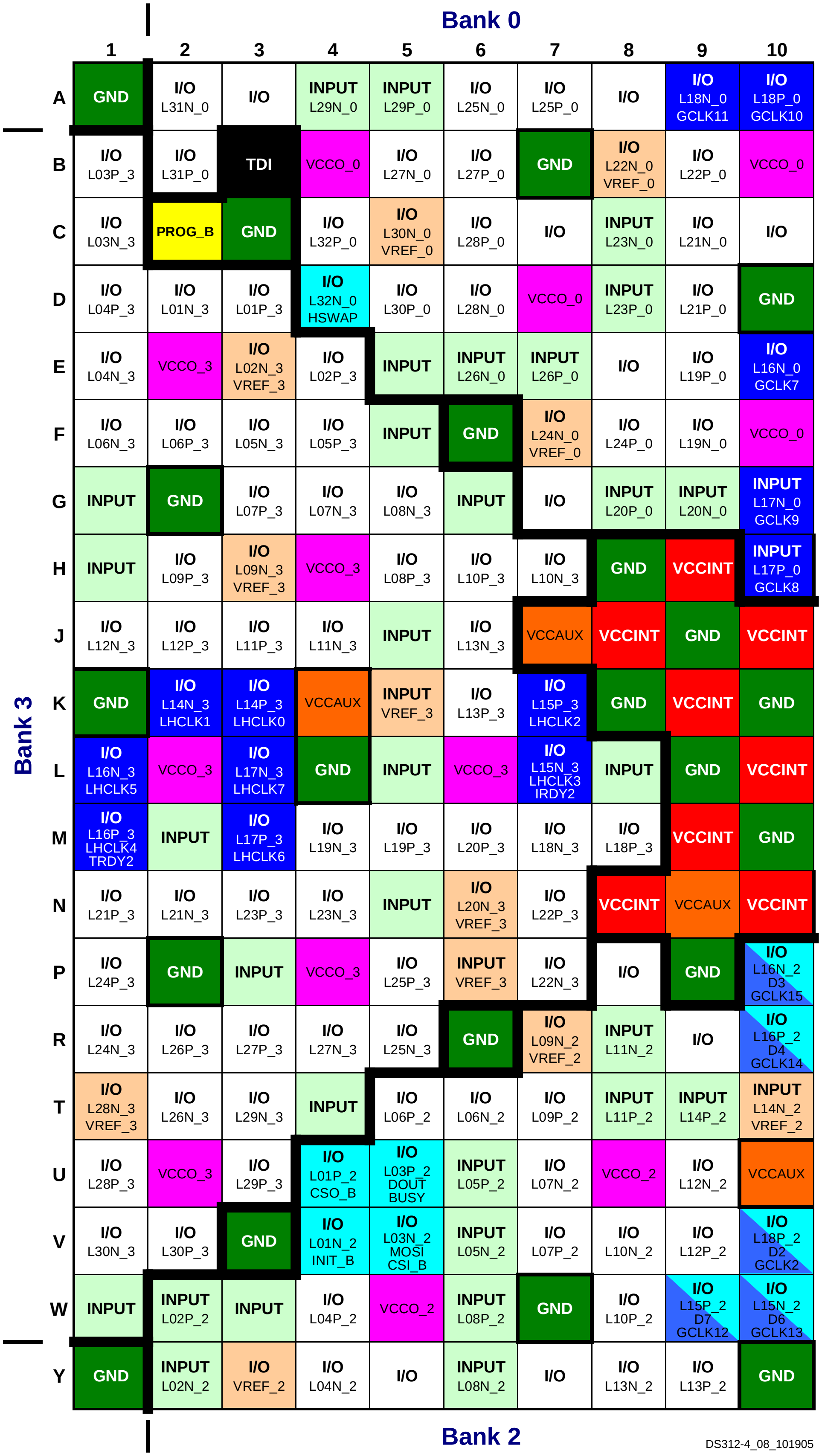
Footprint Migration Differences

The XC3S1200E and XC3S1600E FPGAs have identical footprints in the FG400 package. Designs can migrate between the XC3S1200E and XC3S1600E FPGAs without further consideration.

FG400 Footprint

Left Half of Package (top view)

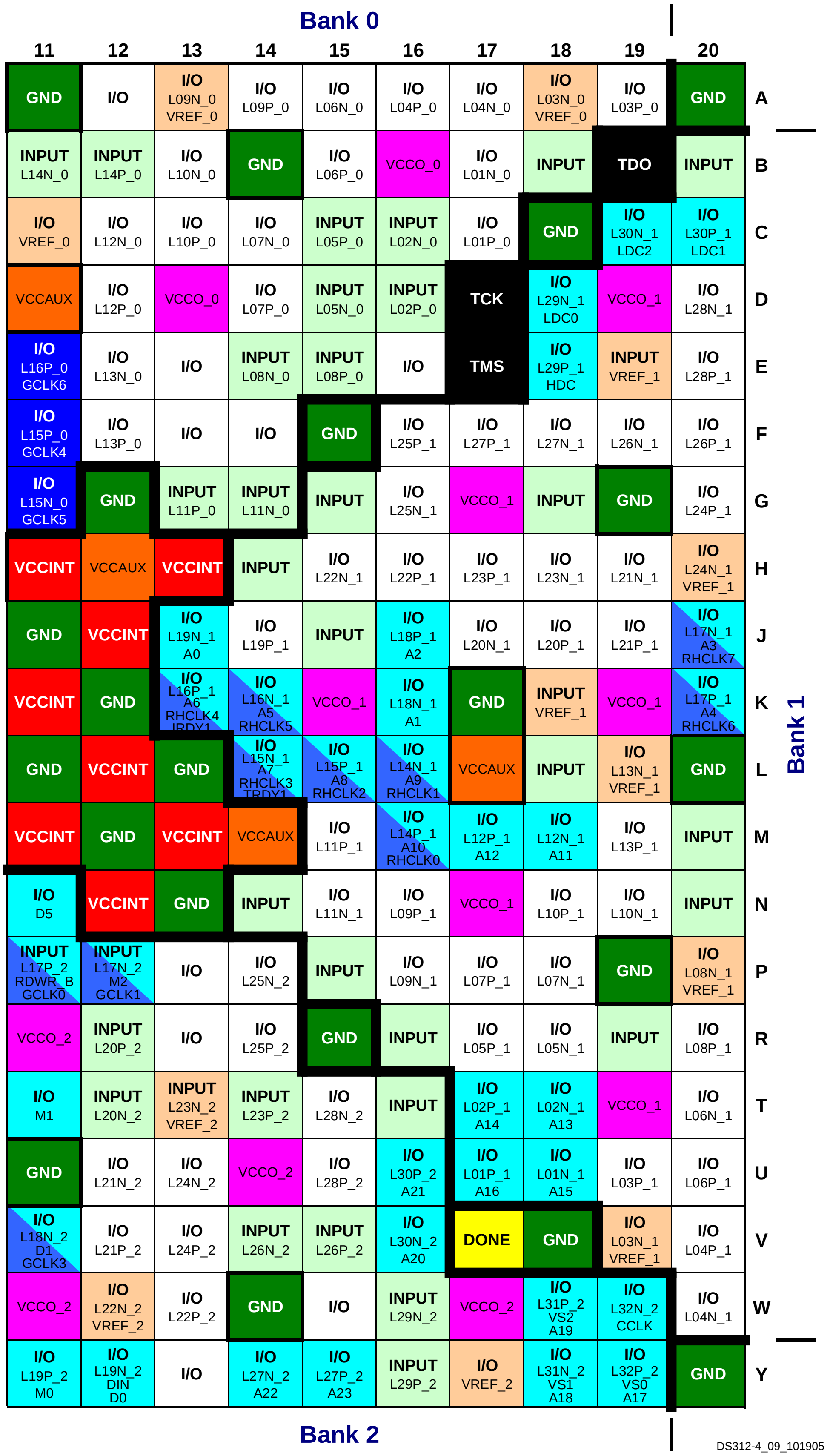
156	**I/O:** Unrestricted, general-purpose user I/O
62	**INPUT:** Unrestricted, general-purpose input pin
46	**DUAL:** Configuration pin, then possible user I/O
24	**VREF:** User I/O or input voltage reference for bank
16	**CLK:** User I/O, input, or clock buffer input
2	**CONFIG:** Dedicated configuration pins
4	**JTAG:** Dedicated JTAG port pins
42	**GND:** Ground
24	**VCCO:** Output voltage supply for bank
16	**VCCINT:** Internal core supply voltage (+1.2V)
8	**VCCAUX:** Auxiliary supply voltage (+2.5V)
0	**N.C.:** Not connected



	1	2	3	4	5	6	7	8	9	10
A	GND	I/O L31N_0	I/O	INPUT L29N_0	INPUT L29P_0	I/O L25N_0	I/O L25P_0	I/O	I/O L18N_0 GCLK11	I/O L18P_0 GCLK10
B	I/O L03P_3	I/O L31P_0	TDI	VCCO_0	I/O L27N_0	I/O L27P_0	GND	I/O L22N_0 VREF_0	I/O L22P_0	VCCO_0
C	I/O L03N_3	PROG_B	GND	I/O L32P_0	I/O L30N_0 VREF_0	I/O L28P_0	I/O	INPUT L23N_0	I/O L21N_0	I/O
D	I/O L04P_3	I/O L01N_3	I/O L01P_3	I/O L32N_0 HSWAP	I/O L30P_0	I/O L28N_0	VCCO_0	INPUT L23P_0	I/O L21P_0	GND
E	I/O L04N_3	VCCO_3	I/O L02N_3 VREF_3	I/O L02P_3	INPUT	INPUT L26N_0	INPUT L26P_0	I/O	I/O L19P_0	I/O L16N_0 GCLK7
F	I/O L06N_3	I/O L06P_3	I/O L05N_3	I/O L05P_3	INPUT	GND	I/O L24N_0 VREF_0	I/O L24P_0	I/O L19N_0	VCCO_0
G	INPUT	GND	I/O L07P_3	I/O L07N_3	I/O L08N_3	INPUT	I/O	INPUT L20P_0	INPUT L20N_0	INPUT L17N_0 GCLK9
H	INPUT	I/O L09P_3	I/O L09N_3 VREF_3	VCCO_3	I/O L08P_3	I/O L10P_3	I/O L10N_3	GND	VCCINT	INPUT L17P_0 GCLK8
J	I/O L12N_3	I/O L12P_3	I/O L11P_3	I/O L11N_3	INPUT	I/O L13N_3	VCCAUX	VCCINT	GND	VCCINT
K	GND	I/O L14N_3 LHCLK1	I/O L14P_3 LHCLK0	VCCAUX	INPUT VREF_3	I/O L13P_3	I/O L15P_3 LHCLK2	GND	VCCINT	GND
L	I/O L16N_3 LHCLK5	VCCO_3	I/O L17N_3 LHCLK7	GND	INPUT	VCCO_3	I/O L15N_3 LHCLK3 IRDY2	INPUT	GND	VCCINT
M	I/O L16P_3 LHCLK4 TRDY2	INPUT	I/O L17P_3 LHCLK6	I/O L19N_3	I/O L19P_3	I/O L20P_3	I/O L18N_3	I/O L18P_3	VCCINT	GND
N	I/O L21P_3	I/O L21N_3	I/O L23P_3	I/O L23N_3	INPUT	I/O L20N_3 VREF_3	I/O L22P_3	VCCINT	VCCAUX	VCCINT
P	I/O L24P_3	GND	INPUT	VCCO_3	I/O L25P_3	INPUT VREF_3	I/O L22N_3	I/O	GND	I/O L16N_2 D3 GCLK15
R	I/O L24N_3	I/O L26P_3	I/O L27P_3	I/O L27N_3	I/O L25N_3	GND	I/O L09N_2 VREF_2	INPUT L11N_2	I/O	I/O L16P_2 D4 GCLK14
T	I/O L28N_3 VREF_3	I/O L26N_3	I/O L29N_3	INPUT	I/O L06P_2	I/O L06N_2	I/O L09P_2	INPUT L11P_2	INPUT L14P_2	INPUT L14N_2 VREF_2
U	I/O L28P_3	VCCO_3	I/O L29P_3	I/O L01P_2 CSO_B	I/O L03P_2 DOUT BUSY	INPUT L05P_2	I/O L07N_2	VCCO_2	I/O L12N_2	VCCAUX
V	I/O L30N_3	I/O L30P_3	GND	I/O L01N_2 INIT_B	I/O L03N_2 MOSI CSI_B	INPUT L05N_2	I/O L07P_2	I/O L10N_2	I/O L12P_2	I/O L18P_2 D2 GCLK2
W	INPUT	INPUT L02P_2	INPUT	I/O L04P_2	VCCO_2	INPUT L08P_2	GND	I/O L10P_2	I/O L15P_2 D7 GCLK12	I/O L15N_2 D6 GCLK13
Y	GND	INPUT L02N_2	I/O VREF_2	I/O L04N_2	I/O	INPUT L08N_2	I/O	I/O L13N_2	I/O L13P_2	GND

Figure 89: **FG400 Package Footprint (top view)**

Right Half of Package (top view)



11	12	13	14	15	16	17	18	19	20	
GND	I/O	I/O L09N_0 VREF_0	I/O L09P_0	I/O L06N_0	I/O L04P_0	I/O L04N_0	I/O L03N_0 VREF_0	I/O L03P_0	GND	A
INPUT L14N_0	INPUT L14P_0	I/O L10N_0	GND	I/O L06P_0	VCCO_0	I/O L01N_0	INPUT	TDO	INPUT	B
I/O VREF_0	I/O L12N_0	I/O L10P_0	I/O L07N_0	INPUT L05P_0	INPUT L02N_0	I/O L01P_0	GND	I/O L30N_1 LDC2	I/O L30P_1 LDC1	C
VCCAUX	I/O L12P_0	VCCO_0	I/O L07P_0	INPUT L05N_0	INPUT L02P_0	TCK	I/O L29N_1 LDC0	VCCO_1	I/O L28N_1	D
I/O L16P_0 GCLK6	I/O L13N_0	I/O	INPUT L08N_0	INPUT L08P_0	I/O	TMS	I/O L29P_1 HDC	INPUT VREF_1	I/O L28P_1	E
I/O L15P_0 GCLK4	I/O L13P_0	I/O	I/O	GND	I/O L25P_1	I/O L27P_1	I/O L27N_1	I/O L26N_1	I/O L26P_1	F
I/O L15N_0 GCLK5	GND	INPUT L11P_0	INPUT L11N_0	INPUT	I/O L25N_1	VCCO_1	INPUT	GND	I/O L24P_1	G
VCCINT	VCCAUX	VCCINT	INPUT	I/O L22N_1	I/O L22P_1	I/O L23P_1	I/O L23N_1	I/O L21N_1	I/O L24N_1 VREF_1	H
GND	VCCINT	I/O L19N_1 A0	I/O L19P_1	INPUT	I/O L18P_1 A2	I/O L20N_1	I/O L20P_1	I/O L21P_1	I/O L17N_1 A3 RHCLK7	J
VCCINT	GND	I/O L16P_1 A6 RHCLK4 IRDY1	I/O L16N_1 A5 RHCLK5	VCCO_1	I/O L18N_1 A1	GND	INPUT VREF_1	VCCO_1	I/O L17P_1 A4 RHCLK6	K
GND	VCCINT	GND	I/O L15N_1 A7 RHCLK3 TRDY1	I/O L15P_1 A8 RHCLK2	I/O L14N_1 A9 RHCLK1	VCCAUX	INPUT	I/O L13N_1 VREF_1	GND	L
VCCINT	GND	VCCINT	VCCAUX	I/O L11P_1	I/O L14P_1 A10 RHCLK0	I/O L12P_1 A12	I/O L12N_1 A11	I/O L13P_1	INPUT	M
I/O D5	VCCINT	GND	INPUT	I/O L11N_1	I/O L09P_1	VCCO_1	I/O L10P_1	I/O L10N_1	INPUT	N
INPUT L17P_2 RDWR_B GCLK0	INPUT L17N_2 M2 GCLK1	I/O	I/O L25N_2	INPUT	I/O L09N_1	I/O L07P_1	I/O L07N_1	GND	I/O L08N_1 VREF_1	P
VCCO_2	INPUT L20P_2	I/O	I/O L25P_2	GND	INPUT	I/O L05P_1	I/O L05N_1	INPUT	I/O L08P_1	R
I/O M1	INPUT L20N_2	INPUT L23N_2 VREF_2	INPUT L23P_2	I/O L28N_2	INPUT	I/O L02P_1 A14	I/O L02N_1 A13	VCCO_1	I/O L06N_1	T
GND	I/O L21N_2	I/O L24N_2	VCCO_2	I/O L28P_2	I/O L30P_2 A21	I/O L01P_1 A16	I/O L01N_1 A15	I/O L03P_1	I/O L06P_1	U
I/O L18N_2 D1 GCLK3	I/O L21P_2	I/O L24P_2	INPUT L26N_2	INPUT L26P_2	I/O L30N_2 A20	DONE	GND	I/O L03N_1 VREF_1	I/O L04P_1	V
VCCO_2	I/O L22N_2 VREF_2	I/O L22P_2	GND	I/O	INPUT L29N_2	VCCO_2	I/O L31P_2 VS2 A19	I/O L32N_2 CCLK	I/O L04N_1	W
I/O L19P_2 M0	I/O L19N_2 DIN D0	I/O	I/O L27N_2 A22	I/O L27P_2 A23	INPUT L29P_2	I/O VREF_2	I/O L31N_2 VS1 A18	I/O L32P_2 VS0 A17	GND	Y

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FG484: 484-ball Fine-pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FG484, supports the XC3S1600E FPGA.

Table 151 lists all the FG484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/bvdocs/publications/s3e_pin.zip.

Pinout Table

Table 151: **FG484 Package Pinout**

Bank	XC3S1600E Pin Name	FG484 Ball	Type
0	IO	B6	I/O
0	IO	B13	I/O
0	IO	C5	I/O
0	IO	C14	I/O
0	IO	E16	I/O
0	IO	F9	I/O
0	IO	F16	I/O
0	IO	G8	I/O
0	IO	H10	I/O
0	IO	H15	I/O
0	IO	J11	I/O
0	IO/VREF_0	G12	VREF
0	IO_L01N_0	C18	I/O
0	IO_L01P_0	C19	I/O
0	IO_L03N_0/VREF_0	A20	VREF
0	IO_L03P_0	A21	I/O
0	IO_L04N_0	A19	I/O
0	IO_L04P_0	A18	I/O
0	IO_L06N_0	C16	I/O
0	IO_L06P_0	D16	I/O
0	IO_L07N_0	A16	I/O
0	IO_L07P_0	A17	I/O
0	IO_L09N_0/VREF_0	B15	VREF
0	IO_L09P_0	C15	I/O
0	IO_L10N_0	G15	I/O
0	IO_L10P_0	F15	I/O
0	IO_L11N_0	D14	I/O
0	IO_L11P_0	E14	I/O
0	IO_L12N_0/VREF_0	A14	VREF
0	IO_L12P_0	A15	I/O
0	IO_L13N_0	H14	I/O
0	IO_L13P_0	G14	I/O
0	IO_L15N_0	G13	I/O
0	IO_L15P_0	F13	I/O
0	IO_L16N_0	J13	I/O
0	IO_L16P_0	H13	I/O
0	IO_L18N_0/GCLK5	E12	GCLK
0	IO_L18P_0/GCLK4	F12	GCLK
0	IO_L19N_0/GCLK7	C12	GCLK
0	IO_L19P_0/GCLK6	B12	GCLK
0	IO_L21N_0/GCLK11	B11	GCLK
0	IO_L21P_0/GCLK10	C11	GCLK
0	IO_L22N_0	D11	I/O
0	IO_L22P_0	E11	I/O
0	IO_L24N_0	A9	I/O
0	IO_L24P_0	A10	I/O
0	IO_L25N_0/VREF_0	D10	VREF
0	IO_L25P_0	C10	I/O
0	IO_L27N_0	H8	I/O
0	IO_L27P_0	H9	I/O
0	IO_L28N_0	C9	I/O
0	IO_L28P_0	B9	I/O
0	IO_L29N_0	E9	I/O
0	IO_L29P_0	D9	I/O
0	IO_L30N_0	B8	I/O
0	IO_L30P_0	A8	I/O
0	IO_L32N_0/VREF_0	F7	VREF
0	IO_L32P_0	F8	I/O
0	IO_L33N_0	A6	I/O
0	IO_L33P_0	A7	I/O
0	IO_L35N_0	A4	I/O
0	IO_L35P_0	A5	I/O
0	IO_L36N_0	E7	I/O
0	IO_L36P_0	D7	I/O
0	IO_L38N_0/VREF_0	D6	VREF
0	IO_L38P_0	D5	I/O
0	IO_L39N_0	B4	I/O
0	IO_L39P_0	B3	I/O
0	IO_L40N_0/HSWAP	D4	DUAL

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
0	IO_L40P_0	C4	I/O
0	IP	B19	INPUT
0	IP	E6	INPUT
0	IP_L02N_0	D17	INPUT
0	IP_L02P_0	D18	INPUT
0	IP_L05N_0	C17	INPUT
0	IP_L05P_0	B17	INPUT
0	IP_L08N_0	E15	INPUT
0	IP_L08P_0	D15	INPUT
0	IP_L14N_0	D13	INPUT
0	IP_L14P_0	C13	INPUT
0	IP_L17N_0	A12	INPUT
0	IP_L17P_0	A13	INPUT
0	IP_L20N_0/GCLK9	H11	GCLK
0	IP_L20P_0/GCLK8	H12	GCLK
0	IP_L23N_0	F10	INPUT
0	IP_L23P_0	F11	INPUT
0	IP_L26N_0	G9	INPUT
0	IP_L26P_0	G10	INPUT
0	IP_L31N_0	C8	INPUT
0	IP_L31P_0	D8	INPUT
0	IP_L34N_0	C7	INPUT
0	IP_L34P_0	C6	INPUT
0	IP_L37N_0	A3	INPUT
0	IP_L37P_0	A2	INPUT
0	VCCO_0	B5	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	F14	VCCO
0	VCCO_0	G11	VCCO
1	IO_L01N_1/A15	Y22	DUAL
1	IO_L01P_1/A16	AA22	DUAL
1	IO_L02N_1/A13	W21	DUAL
1	IO_L02P_1/A14	Y21	DUAL
1	IO_L03N_1/VREF_1	W20	VREF
1	IO_L03P_1	V20	I/O
1	IO_L04N_1	U19	I/O
1	IO_L04P_1	V19	I/O
1	IO_L05N_1	V22	I/O

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	IO_L05P_1	W22	I/O
1	IO_L06N_1	T19	I/O
1	IO_L06P_1	T18	I/O
1	IO_L07N_1/VREF_1	U20	VREF
1	IO_L07P_1	U21	I/O
1	IO_L08N_1	T22	I/O
1	IO_L08P_1	U22	I/O
1	IO_L09N_1	R19	I/O
1	IO_L09P_1	R18	I/O
1	IO_L10N_1	R16	I/O
1	IO_L10P_1	T16	I/O
1	IO_L11N_1	R21	I/O
1	IO_L11P_1	R20	I/O
1	IO_L12N_1/VREF_1	P18	VREF
1	IO_L12P_1	P17	I/O
1	IO_L13N_1	P22	I/O
1	IO_L13P_1	R22	I/O
1	IO_L14N_1	P15	I/O
1	IO_L14P_1	P16	I/O
1	IO_L15N_1	N18	I/O
1	IO_L15P_1	N19	I/O
1	IO_L16N_1/A11	N16	DUAL
1	IO_L16P_1/A12	N17	DUAL
1	IO_L17N_1/VREF_1	M20	VREF
1	IO_L17P_1	N20	I/O
1	IO_L18N_1/A9/RHCLK1	M22	RHCLK/ DUAL
1	IO_L18P_1/A10/RHCLK0	N22	RHCLK/ DUAL
1	IO_L19N_1/A7/RHCLK3/ TRDY1	M16	RHCLK/ DUAL
1	IO_L19P_1/A8/RHCLK2	M15	RHCLK/ DUAL
1	IO_L20N_1/A5/RHCLK5	L21	RHCLK/ DUAL
1	IO_L20P_1/A6/RHCLK4/ IRDY1	L20	RHCLK/ DUAL
1	IO_L21N_1/A3/RHCLK7	L19	RHCLK/ DUAL
1	IO_L21P_1/A4/RHCLK6	L18	RHCLK/ DUAL
1	IO_L22N_1/A1	K22	DUAL
1	IO_L22P_1/A2	L22	DUAL

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	IO_L23N_1/A0	K17	DUAL
1	IO_L23P_1	K16	I/O
1	IO_L24N_1	K19	I/O
1	IO_L24P_1	K18	I/O
1	IO_L25N_1	K15	I/O
1	IO_L25P_1	J15	I/O
1	IO_L26N_1	J20	I/O
1	IO_L26P_1	J21	I/O
1	IO_L27N_1	J17	I/O
1	IO_L27P_1	J18	I/O
1	IO_L28N_1/VREF_1	H21	VREF
1	IO_L28P_1	H22	I/O
1	IO_L29N_1	H20	I/O
1	IO_L29P_1	H19	I/O
1	IO_L30N_1	H17	I/O
1	IO_L30P_1	G17	I/O
1	IO_L31N_1	F22	I/O
1	IO_L31P_1	G22	I/O
1	IO_L32N_1	F20	I/O
1	IO_L32P_1	G20	I/O
1	IO_L33N_1	G18	I/O
1	IO_L33P_1	G19	I/O
1	IO_L34N_1	D22	I/O
1	IO_L34P_1	E22	I/O
1	IO_L35N_1	F19	I/O
1	IO_L35P_1	F18	I/O
1	IO_L36N_1	E20	I/O
1	IO_L36P_1	E19	I/O
1	IO_L37N_1/LDC0	C21	DUAL
1	IO_L37P_1/HDC	C22	DUAL
1	IO_L38N_1/LDC2	B21	DUAL
1	IO_L38P_1/LDC1	B22	DUAL
1	IP	D20	INPUT
1	IP	F21	INPUT
1	IP	G16	INPUT
1	IP	H16	INPUT
1	IP	J16	INPUT
1	IP	J22	INPUT
1	IP	K20	INPUT
1	IP	L15	INPUT
1	IP	M18	INPUT

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	IP	N15	INPUT
1	IP	N21	INPUT
1	IP	P20	INPUT
1	IP	R15	INPUT
1	IP	T17	INPUT
1	IP	T20	INPUT
1	IP	U18	INPUT
1	IP/VREF_1	D21	VREF
1	IP/VREF_1	L17	VREF
1	VCCO_1	E21	VCCO
1	VCCO_1	H18	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	L16	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	R17	VCCO
1	VCCO_1	V21	VCCO
2	IO	Y8	I/O
2	IO	Y9	I/O
2	IO	AA10	I/O
2	IO	AB5	I/O
2	IO	AB13	I/O
2	IO	AB14	I/O
2	IO	AB16	I/O
2	IO	AB18	I/O
2	IO/D5	AB11	DUAL
2	IO/M1	AA12	DUAL
2	IO/VREF_2	AB4	VREF
2	IO/VREF_2	AB21	VREF
2	IO_L01N_2/INIT_B	AB3	DUAL
2	IO_L01P_2/CSO_B	AA3	DUAL
2	IO_L03N_2/MOSI/CSI_B	Y5	DUAL
2	IO_L03P_2/DOUT/BUSY	W5	DUAL
2	IO_L04N_2	W6	I/O
2	IO_L04P_2	V6	I/O
2	IO_L06N_2	W7	I/O
2	IO_L06P_2	Y7	I/O
2	IO_L07N_2	U7	I/O
2	IO_L07P_2	V7	I/O
2	IO_L09N_2/VREF_2	V8	VREF
2	IO_L09P_2	W8	I/O
2	IO_L10N_2	T8	I/O

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IO_L10P_2	U8	I/O
2	IO_L11N_2	AB8	I/O
2	IO_L11P_2	AA8	I/O
2	IO_L12N_2	W9	I/O
2	IO_L12P_2	V9	I/O
2	IO_L13N_2/VREF_2	R9	VREF
2	IO_L13P_2	T9	I/O
2	IO_L14N_2	AB9	I/O
2	IO_L14P_2	AB10	I/O
2	IO_L16N_2	U10	I/O
2	IO_L16P_2	T10	I/O
2	IO_L17N_2	R10	I/O
2	IO_L17P_2	P10	I/O
2	IO_L19N_2/D6/GCLK13	U11	DUAL/ GCLK
2	IO_L19P_2/D7/GCLK12	V11	DUAL/ GCLK
2	IO_L20N_2/D3/GCLK15	T11	DUAL/ GCLK
2	IO_L20P_2/D4/GCLK14	R11	DUAL/ GCLK
2	IO_L22N_2/D1/GCLK3	W12	DUAL/ GCLK
2	IO_L22P_2/D2/GCLK2	Y12	DUAL/ GCLK
2	IO_L23N_2/DIN/D0	U12	DUAL
2	IO_L23P_2/M0	V12	DUAL
2	IO_L25N_2	Y13	I/O
2	IO_L25P_2	W13	I/O
2	IO_L26N_2/VREF_2	U14	VREF
2	IO_L26P_2	U13	I/O
2	IO_L27N_2	T14	I/O
2	IO_L27P_2	R14	I/O
2	IO_L28N_2	Y14	I/O
2	IO_L28P_2	AA14	I/O
2	IO_L29N_2	W14	I/O
2	IO_L29P_2	V14	I/O
2	IO_L30N_2	AB15	I/O
2	IO_L30P_2	AA15	I/O
2	IO_L32N_2	W15	I/O
2	IO_L32P_2	Y15	I/O
2	IO_L33N_2	U16	I/O
2	IO_L33P_2	V16	I/O

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IO_L35N_2/A22	AB17	DUAL
2	IO_L35P_2/A23	AA17	DUAL
2	IO_L36N_2	W17	I/O
2	IO_L36P_2	Y17	I/O
2	IO_L38N_2/A20	Y18	DUAL
2	IO_L38P_2/A21	W18	DUAL
2	IO_L39N_2/VS1/A18	AA20	DUAL
2	IO_L39P_2/VS2/A19	AB20	DUAL
2	IO_L40N_2/CCLK	W19	DUAL
2	IO_L40P_2/VS0/A17	Y19	DUAL
2	IP	V17	INPUT
2	IP	AB2	INPUT
2	IP_L02N_2	AA4	INPUT
2	IP_L02P_2	Y4	INPUT
2	IP_L05N_2	Y6	INPUT
2	IP_L05P_2	AA6	INPUT
2	IP_L08N_2	AB7	INPUT
2	IP_L08P_2	AB6	INPUT
2	IP_L15N_2	Y10	INPUT
2	IP_L15P_2	W10	INPUT
2	IP_L18N_2/VREF_2	AA11	VREF
2	IP_L18P_2	Y11	INPUT
2	IP_L21N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L21P_2/RDWR_B/ GCLK0	R12	DUAL/ GCLK
2	IP_L24N_2	R13	INPUT
2	IP_L24P_2	T13	INPUT
2	IP_L31N_2/VREF_2	T15	VREF
2	IP_L31P_2	U15	INPUT
2	IP_L34N_2	Y16	INPUT
2	IP_L34P_2	W16	INPUT
2	IP_L37N_2	AA19	INPUT
2	IP_L37P_2	AB19	INPUT
2	VCCO_2	T12	VCCO
2	VCCO_2	U9	VCCO
2	VCCO_2	V15	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
3	IO_L01N_3	C1	I/O

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
3	IO_L01P_3	C2	I/O
3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	D3	I/O
3	IO_L03N_3	E3	I/O
3	IO_L03P_3	E4	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F4	I/O
3	IO_L05P_3	F3	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	G4	I/O
3	IO_L07N_3	F1	I/O
3	IO_L07P_3	G1	I/O
3	IO_L08N_3/VREF_3	G6	VREF
3	IO_L08P_3	G7	I/O
3	IO_L09N_3	H4	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	H2	I/O
3	IO_L10P_3	H3	I/O
3	IO_L11N_3	H1	I/O
3	IO_L11P_3	J1	I/O
3	IO_L12N_3	J6	I/O
3	IO_L12P_3	J5	I/O
3	IO_L13N_3/VREF_3	J3	VREF
3	IO_L13P_3	K3	I/O
3	IO_L14N_3	J8	I/O
3	IO_L14P_3	K8	I/O
3	IO_L15N_3	K4	I/O
3	IO_L15P_3	K5	I/O
3	IO_L16N_3	K1	I/O
3	IO_L16P_3	L1	I/O
3	IO_L17N_3	L7	I/O
3	IO_L17P_3	K7	I/O
3	IO_L18N_3/LHCLK1	L5	LHCLK
3	IO_L18P_3/LHCLK0	M5	LHCLK
3	IO_L19N_3/LHCLK3/IRDY2	M8	LHCLK
3	IO_L19P_3/LHCLK2	L8	LHCLK
3	IO_L20N_3/LHCLK5	N1	LHCLK
3	IO_L20P_3/LHCLK4/TRDY2	M1	LHCLK
3	IO_L21N_3/LHCLK7	M4	LHCLK
3	IO_L21P_3/LHCLK6	M3	LHCLK

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
3	IO_L22N_3	N6	I/O
3	IO_L22P_3	N7	I/O
3	IO_L23N_3	P8	I/O
3	IO_L23P_3	N8	I/O
3	IO_L24N_3/VREF_3	N4	VREF
3	IO_L24P_3	N5	I/O
3	IO_L25N_3	P2	I/O
3	IO_L25P_3	P1	I/O
3	IO_L26N_3	R7	I/O
3	IO_L26P_3	P7	I/O
3	IO_L27N_3	P6	I/O
3	IO_L27P_3	P5	I/O
3	IO_L28N_3	R2	I/O
3	IO_L28P_3	R1	I/O
3	IO_L29N_3	R3	I/O
3	IO_L29P_3	R4	I/O
3	IO_L30N_3	T6	I/O
3	IO_L30P_3	R6	I/O
3	IO_L31N_3	U2	I/O
3	IO_L31P_3	U1	I/O
3	IO_L32N_3	T4	I/O
3	IO_L32P_3	T5	I/O
3	IO_L33N_3	W1	I/O
3	IO_L33P_3	V1	I/O
3	IO_L34N_3	U4	I/O
3	IO_L34P_3	U3	I/O
3	IO_L35N_3	V4	I/O
3	IO_L35P_3	V3	I/O
3	IO_L36N_3/VREF_3	W3	VREF
3	IO_L36P_3	W2	I/O
3	IO_L37N_3	Y2	I/O
3	IO_L37P_3	Y1	I/O
3	IO_L38N_3	AA1	I/O
3	IO_L38P_3	AA2	I/O
3	IP	F2	INPUT
3	IP	F5	INPUT
3	IP	G3	INPUT
3	IP	H7	INPUT
3	IP	J7	INPUT
3	IP	K2	INPUT
3	IP	K6	INPUT

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
3	IP	M2	INPUT
3	IP	M6	INPUT
3	IP	N3	INPUT
3	IP	P3	INPUT
3	IP	R8	INPUT
3	IP	T1	INPUT
3	IP	T7	INPUT
3	IP	U5	INPUT
3	IP	W4	INPUT
3	IP/VREF_3	L3	VREF
3	IP/VREF_3	T3	VREF
3	VCCO_3	E2	VCCO
3	VCCO_3	H6	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	M7	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	R5	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A22	GND
GND	GND	B7	GND
GND	GND	B16	GND
GND	GND	C3	GND
GND	GND	C20	GND
GND	GND	E10	GND
GND	GND	E13	GND
GND	GND	F6	GND
GND	GND	F17	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	J12	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
GND	GND	L13	GND
GND	GND	M10	GND
GND	GND	M14	GND
GND	GND	M17	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	P11	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U6	GND
GND	GND	U17	GND
GND	GND	V10	GND
GND	GND	V13	GND
GND	GND	Y3	GND
GND	GND	Y20	GND
GND	GND	AA7	GND
GND	GND	AA16	GND
GND	GND	AB1	GND
GND	GND	AB12	GND
GND	GND	AB22	GND
VCCAUX	DONE	AA21	CONFIG
VCCAUX	PROG_B	B1	CONFIG
VCCAUX	TCK	E17	JTAG
VCCAUX	TDI	B2	JTAG
VCCAUX	TDO	B20	JTAG
VCCAUX	TMS	D19	JTAG
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	K14	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	N9	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX
VCCAUX	VCCAUX	W11	VCCAUX

Table 151: **FG484 Package Pinout *(Continued)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L11	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M12	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P13	VCCINT

User I/Os by Bank

Table 152 indicates how the 304 available user-I/O pins are distributed between the four I/O banks on the FG484 package.

Table 152: **User I/Os Per Bank for the XC3S1600E in the FG484 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	94	56	22	1	7	8
Right	1	94	50	16	21	7	0[1]
Bottom	2	94	45	18	24	7	0[1]
Left	3	94	63	16	0	7	8
TOTAL		**376**	**214**	**72**	**46**	**28**	**16**

Notes:

1. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

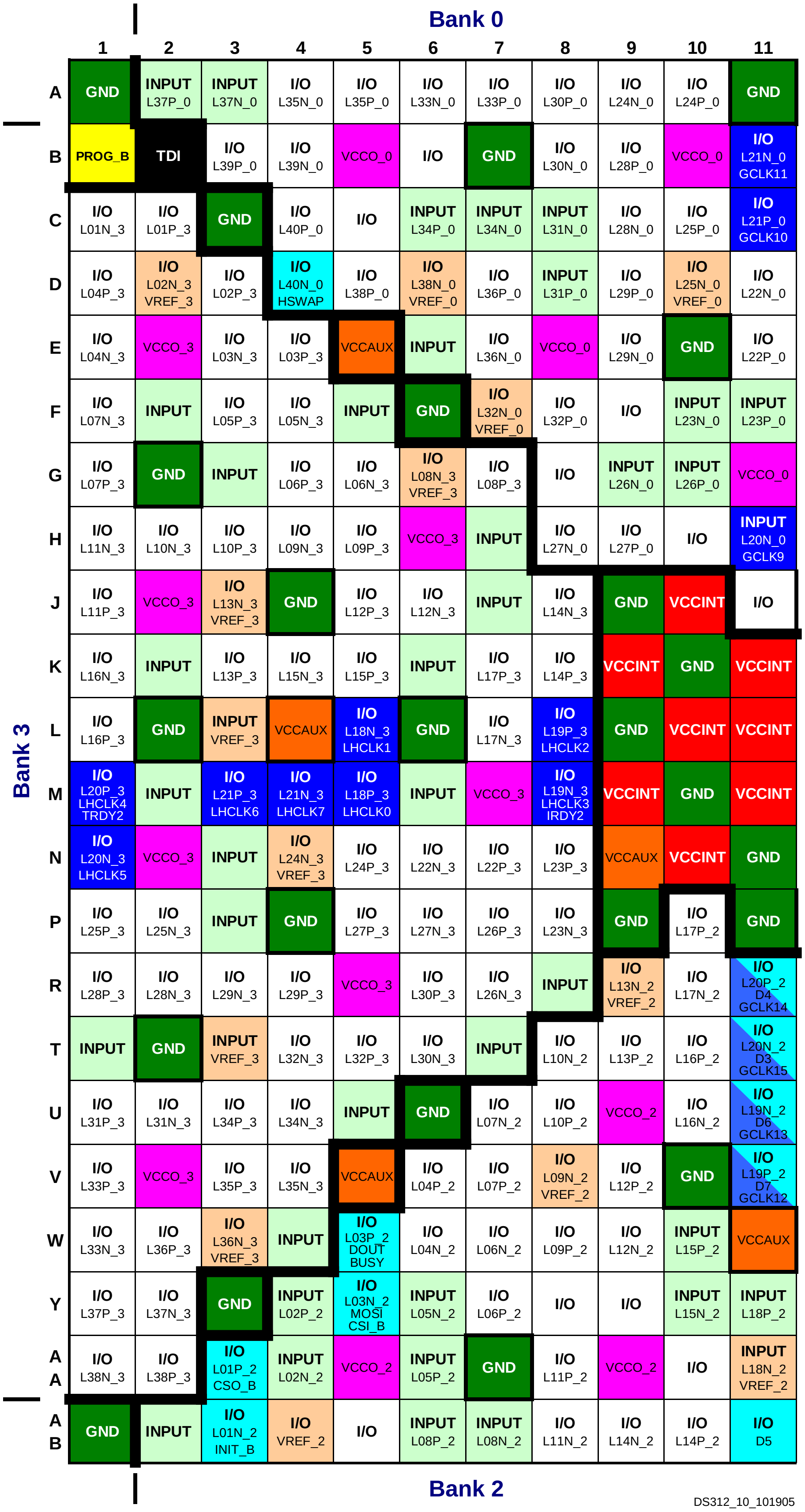
Footprint Migration Differences

The XC3S1600E FPGA is the only Spartan-3E device offered in the FG484 package.

FG484 Footprint

Left Half of Package (top view)

214	**I/O:** Unrestricted, general-purpose user I/O
72	**INPUT:** User I/O or reference resistor input for bank
46	**DUAL:** Configuration pin, then possible user I/O
28	**VREF:** User I/O or input voltage reference for bank
16	**CLK:** User I/O, input, or clock buffer input
2	**CONFIG:** Dedicated configuration pins
4	**JTAG:** Dedicated JTAG port pins
48	**GND:** Ground
28	**VCCO:** Output voltage supply for bank
16	**VCCINT:** Internal core supply voltage (+1.2V)
10	**VCCAUX:** Auxiliary supply voltage (+2.5V)
0	**N.C.:** Not connected



Bank 0

Bank 3

	1	2	3	4	5	6	7	8	9	10	11
A	GND	INPUT L37P_0	INPUT L37N_0	I/O L35N_0	I/O L35P_0	I/O L33N_0	I/O L33P_0	I/O L30P_0	I/O L24N_0	I/O L24P_0	GND
B	PROG_B	TDI	I/O L39P_0	I/O L39N_0	VCCO_0	I/O	GND	I/O L30N_0	I/O L28P_0	VCCO_0	I/O L21N_0 GCLK11
C	I/O L01N_3	I/O L01P_3	GND	I/O L40P_0	I/O	INPUT L34P_0	INPUT L34N_0	INPUT L31N_0	I/O L28N_0	I/O L25P_0	I/O L21P_0 GCLK10
D	I/O L04P_3	I/O L02N_3 VREF_3	I/O L02P_3	I/O L40N_0 HSWAP	I/O L38P_0	I/O L38N_0 VREF_0	I/O L36P_0	INPUT L31P_0	I/O L29P_0	I/O L25N_0 VREF_0	I/O L22N_0
E	I/O L04N_3	VCCO_3	I/O L03N_3	I/O L03P_3	VCCAUX	INPUT	I/O L36N_0	VCCO_0	I/O L29N_0	GND	I/O L22P_0
F	I/O L07N_3	INPUT	I/O L05P_3	I/O L05N_3	INPUT	GND	I/O L32N_0 VREF_0	I/O L32P_0	I/O	INPUT L23N_0	INPUT L23P_0
G	I/O L07P_3	GND	INPUT	I/O L06P_3	I/O L06N_3	I/O L08N_3 VREF_3	I/O L08P_3	I/O	INPUT L26N_0	INPUT L26P_0	VCCO_0
H	I/O L11N_3	I/O L10N_3	I/O L10P_3	I/O L09N_3	I/O L09P_3	VCCO_3	INPUT	I/O L27N_0	I/O L27P_0	I/O	INPUT L20N_0 GCLK9
J	I/O L11P_3	VCCO_3	I/O L13N_3 VREF_3	GND	I/O L12P_3	I/O L12N_3	INPUT	I/O L14N_3	GND	VCCINT	I/O
K	I/O L16N_3	INPUT	I/O L13P_3	I/O L15N_3	I/O L15P_3	INPUT	I/O L17P_3	I/O L14P_3	VCCINT	GND	VCCINT
L	I/O L16P_3	GND	INPUT VREF_3	VCCAUX	I/O L18N_3 LHCLK1	GND	I/O L17N_3	I/O L19P_3 LHCLK2	GND	VCCINT	VCCINT
M	I/O L20P_3 LHCLK4 TRDY2	INPUT	I/O L21P_3 LHCLK6	I/O L21N_3 LHCLK7	I/O L18P_3 LHCLK0	INPUT	VCCO_3	I/O L19N_3 LHCLK3 IRDY2	VCCINT	GND	VCCINT
N	I/O L20N_3 LHCLK5	VCCO_3	INPUT	I/O L24N_3 VREF_3	I/O L24P_3	I/O L22N_3	I/O L22P_3	I/O L23P_3	VCCAUX	VCCINT	GND
P	I/O L25P_3	I/O L25N_3	INPUT	GND	I/O L27P_3	I/O L27N_3	I/O L26P_3	I/O L23N_3	GND	I/O L17P_2	GND
R	I/O L28P_3	I/O L28N_3	I/O L29N_3	I/O L29P_3	VCCO_3	I/O L30P_3	I/O L26N_3	INPUT	I/O L13N_2 VREF_2	I/O L17N_2	I/O L20P_2 D4 GCLK14
T	INPUT	GND	INPUT VREF_3	I/O L32N_3	I/O L32P_3	I/O L30N_3	INPUT	I/O L10N_2	I/O L13P_2	I/O L16P_2	I/O L20N_2 D3 GCLK15
U	I/O L31P_3	I/O L31N_3	I/O L34P_3	I/O L34N_3	INPUT	GND	I/O L07N_2	I/O L10P_2	VCCO_2	I/O L16N_2	I/O L19N_2 D6 GCLK13
V	I/O L33P_3	VCCO_3	I/O L35P_3	I/O L35N_3	VCCAUX	I/O L04P_2	I/O L07P_2	I/O L09N_2 VREF_2	I/O L12P_2	GND	I/O L19P_2 D7 GCLK12
W	I/O L33N_3	I/O L36P_3	I/O L36N_3 VREF_3	INPUT	I/O L03P_2 DOUT BUSY	I/O L04N_2	I/O L06N_2	I/O L09P_2	I/O L12N_2	INPUT L15P_2	VCCAUX
Y	I/O L37P_3	I/O L37N_3	GND	INPUT L02P_2	I/O L03N_2 MOSI CSI_B	INPUT L05N_2	I/O L06P_2	I/O	I/O	INPUT L15N_2	INPUT L18P_2
AA	I/O L38N_3	I/O L38P_3	I/O L01P_2 CSO_B	INPUT L02N_2	VCCO_2	INPUT L05P_2	GND	I/O L11P_2	VCCO_2	I/O	INPUT L18N_2 VREF_2
AB	GND	INPUT	I/O L01N_2 INIT_B	I/O VREF_2	I/O	INPUT L08P_2	INPUT L08N_2	I/O L11N_2	I/O L14N_2	I/O L14P_2	I/O D5

Bank 2

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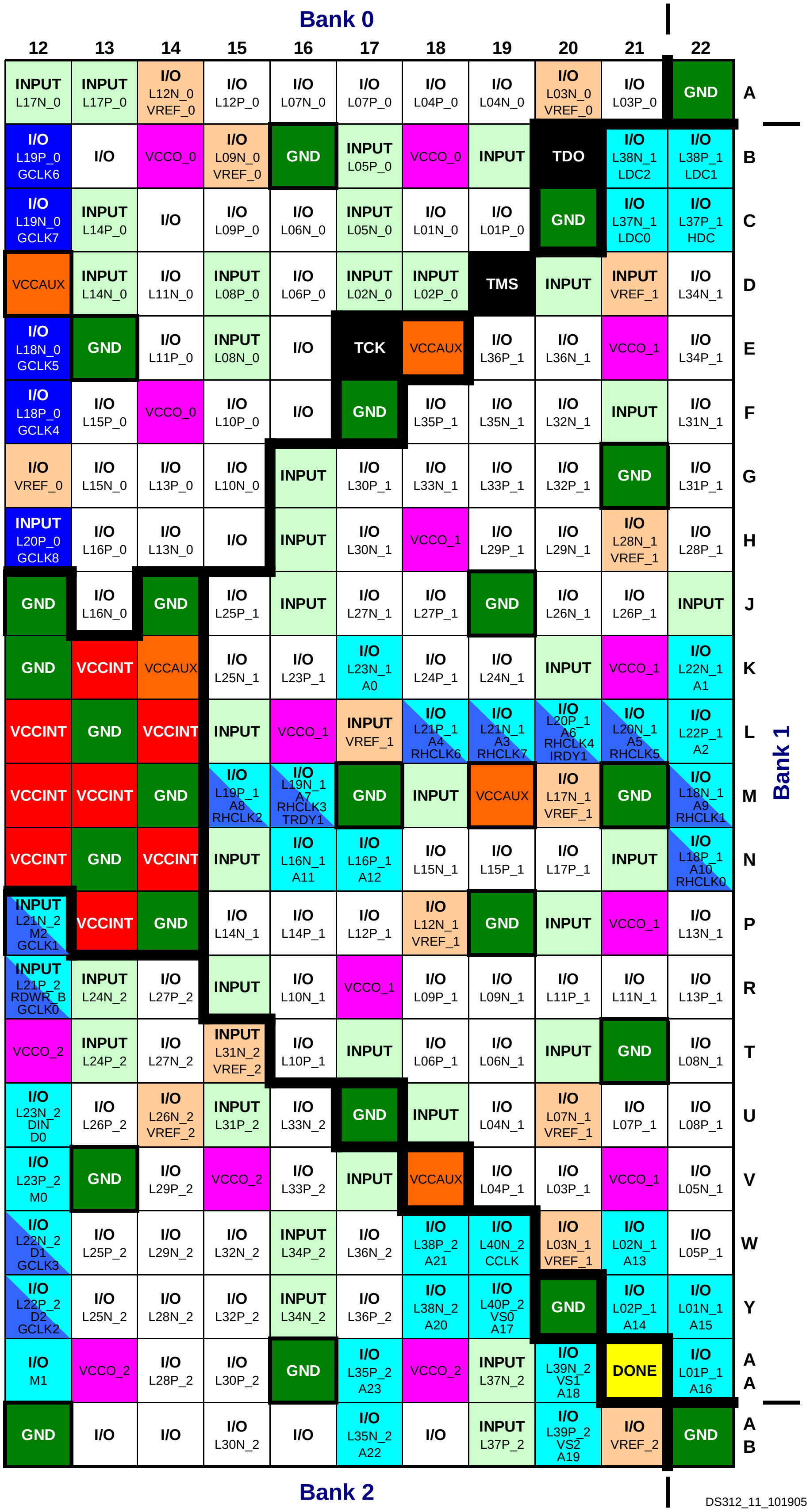
Figure 90: **FG484 Package Footprint (top view)**

Right Half of Package (top view)



Bank 0

12	13	14	15	16	17	18	19	20	21	22	
INPUT L17N_0	INPUT L17P_0	I/O L12N_0 VREF_0	I/O L12P_0	I/O L07N_0	I/O L07P_0	I/O L04P_0	I/O L04N_0	I/O L03N_0 VREF_0	I/O L03P_0	GND	A
I/O L19P_0 GCLK6	I/O	VCCO_0	I/O L09N_0 VREF_0	GND	INPUT L05P_0	VCCO_0	INPUT	TDO	I/O L38N_1 LDC2	I/O L38P_1 LDC1	B
I/O L19N_0 GCLK7	INPUT L14P_0	I/O	I/O L09P_0	I/O L06N_0	INPUT L05N_0	I/O L01N_0	I/O L01P_0	GND	I/O L37N_1 LDC0	I/O L37P_1 HDC	C
VCCAUX	INPUT L14N_0	I/O L11N_0	INPUT L08P_0	I/O L06P_0	INPUT L02N_0	INPUT L02P_0	TMS	INPUT	INPUT VREF_1	I/O L34N_1	D
I/O L18N_0 GCLK5	GND	I/O L11P_0	INPUT L08N_0	I/O	TCK	VCCAUX	I/O L36P_1	I/O L36N_1	VCCO_1	I/O L34P_1	E
I/O L18P_0 GCLK4	I/O L15P_0	VCCO_0	I/O L10P_0	I/O	GND	I/O L35P_1	I/O L35N_1	I/O L32N_1	INPUT	I/O L31N_1	F
I/O VREF_0	I/O L15N_0	I/O L13P_0	I/O L10N_0	INPUT	I/O L30P_1	I/O L33N_1	I/O L33P_1	I/O L32P_1	GND	I/O L31P_1	G
INPUT L20P_0 GCLK8	I/O L16P_0	I/O L13N_0	I/O	INPUT	I/O L30N_1	VCCO_1	I/O L29P_1	I/O L29N_1	I/O L28N_1 VREF_1	I/O L28P_1	H
GND	I/O L16N_0	GND	I/O L25P_1	INPUT	I/O L27N_1	I/O L27P_1	GND	I/O L26N_1	I/O L26P_1	INPUT	J
GND	VCCINT	VCCAUX	I/O L25N_1	I/O L23P_1	I/O L23N_1 A0	I/O L24P_1	I/O L24N_1	INPUT	VCCO_1	I/O L22N_1 A1	K
VCCINT	GND	VCCINT	INPUT	VCCO_1	INPUT VREF_1	I/O L21P_1 A4 RHCLK6	I/O L21N_1 A3 RHCLK7	I/O L20P_1 A6 RHCLK4 IRDY1	I/O L20N_1 A5 RHCLK5	I/O L22P_1 A2	L
VCCINT	VCCINT	GND	I/O L19P_1 A8 RHCLK2	I/O L19N_1 A7 RHCLK3 TRDY1	GND	INPUT	VCCAUX	I/O L17N_1 VREF_1	GND	I/O L18N_1 A9 RHCLK1	M
VCCINT	GND	VCCINT	INPUT	I/O L16N_1 A11	I/O L16P_1 A12	I/O L15N_1	I/O L15P_1	I/O L17P_1	INPUT	I/O L18P_1 A10 RHCLK0	N
INPUT L21N_2 M2 GCLK1	VCCINT	GND	I/O L14N_1	I/O L14P_1	I/O L12P_1	I/O L12N_1 VREF_1	GND	INPUT	VCCO_1	I/O L13N_1	P
INPUT L21P_2 RDWR_B GCLK0	INPUT L24N_2	I/O L27P_2	INPUT	I/O L10N_1	VCCO_1	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	I/O L13P_1	R
VCCO_2	INPUT L24P_2	I/O L27N_2	INPUT L31N_2 VREF_2	I/O L10P_1	INPUT	I/O L06P_1	I/O L06N_1	INPUT	GND	I/O L08N_1	T
I/O L23N_2 DIN D0	I/O L26P_2	I/O L26N_2 VREF_2	INPUT L31P_2	I/O L33N_2	GND	INPUT	I/O L04N_1	I/O L07N_1 VREF_1	I/O L07P_1	I/O L08P_1	U
I/O L23P_2 M0	GND	I/O L29P_2	VCCO_2	I/O L33P_2	INPUT	VCCAUX	I/O L04P_1	I/O L03P_1	VCCO_1	I/O L05N_1	V
I/O L22N_2 D1 GCLK3	I/O L25P_2	I/O L29N_2	I/O L32N_2	INPUT L34P_2	I/O L36N_2	I/O L38P_2 A21	I/O L40N_2 CCLK	I/O L03N_1 VREF_1	I/O L02N_1 A13	I/O L05P_1	W
I/O L22P_2 D2 GCLK2	I/O L25N_2	I/O L28N_2	I/O L32P_2	INPUT L34N_2	I/O L36P_2	I/O L38N_2 A20	I/O L40P_2 VS0 A17	GND	I/O L02P_1 A14	I/O L01N_1 A15	Y
I/O M1	VCCO_2	I/O L28P_2	I/O L30P_2	GND	I/O L35P_2 A23	VCCO_2	INPUT L37N_2	I/O L39N_2 VS1 A18	DONE	I/O L01P_1 A16	AA
GND	I/O	I/O	I/O L30N_2	I/O	I/O L35N_2 A22	I/O	INPUT L37P_2	I/O L39P_2 VS2 A19	I/O VREF_2	GND	AB

Bank 1

Bank 2

DS312_11_101905

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in the CP132 package to Table 126. Corrected number of differential I/O pairs on CP132. Added pinout and footprint information for the CP132, FG400, and FG484 packages. Removed IRDY and TRDY pins from the VQ100, TQ144, and PQ208 packages.
11/23/05	2.0	Corrected title of Table 150. Updated differential pair numbering for some pins in Bank 0 of the FG400 package, affecting Table 149 and Figure 89. Pin functionality and ball assignment were not affected. Added **Package Thermal Characteristics** section. Added package mass values to Table 122.
03/22/06	3.0	Included I/O pins, not just input-only pins under the VREF description in Table 121. Clarified that some global clock inputs are Input-only pins in Table 121. Added information on the XC3S100E in the CP132 package, affecting Table 126, Table 127, Table 130, Table 131, Table 133, and Figure 83. Ball A12 on the XC3S1600E in the FG320 package a full I/O pin, not an Input-only pin. Corrected the I/O counts for the XC3S1600E in the FG320 package, affecting Table 126, Table 147, Table 148, and Figure 88. Corrected pin type for XC3S1600E balls N14 and N15 in Table 145.
05/19/06	3.1	Minor text edits.