TEAC FD-05HF-8630
MICRO FLOPPY DISK DRIVE

SPECIFICATION

Pre-Rev. A

5564

30 sheets in Total

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1. OUTLINE

This specification provides a description for the TEAC FD-05HF, dual density (2/1MB, 2-modes), half inch high, 90mm (3.5-inch) micro floppy disk drive (hereinafter referred to as the FDD). Table 1-1 shows the outline of the FDD, and Table 1-2 shows the signal interface pin-assignment.

(Table 1-1) Specification outline

Model name	FD-05HF-8630	
Front bezel	Black	
Flap	Black	
Eject button	Black	
LED indicator	Green	
Safety standard	UL, CSA & TÜV	
Operation modes	2MB mode Write and read	1MB mode Write and read
90mm (3.5-inch) disk used	High density (2HD)	Normal density (2DD)
Unformatted data capacity	2M bytes	1M bytes
Data transfer rate	500k bits/s	250k bits/s
Disk rotational speed	300rpm	300rpm
Track density	5.3track/mm (135tpi)	
Track to track time	3ms	
Required power	+5V single (4.5 ~ 5.5V)	
Signal output driver	CMOS, 3-state	
Input signal pull-up	20kΩ ±50%, unremovable	
Function	1. Pin 6 : DISK CHANGE output Pin 8 : READY output Pin 9 : HD OUT output 2. Automatic density setting for 2DD (1MB) disk or 2HD (1.6M/ 2MB) disk. 3. Ready and seek-complete gate (full-mask) for INDEX and READ DATA output pulses. 4. LED turns on at DRIVE SELECTed and ready. 5. Equipped with auto-recalibration. 6. No auto-chucking. 7. 26pin (1mm pitch) straight ZIF connector for FFC or FPC including power.	
Other optional function & mechanism	Equipped with cover L.	

(Table 1-2) Signal interface pin-assignment

Pin Nos.	Signals	Pin Nos.	Signals
1	+5V	2	INDEX
3	+5V	4	DRIVE SELECT
5	+5V	6	DISK CHANGE
7	NC	8	READY
9	HD OUT (HD at HIGH level)	10	MOTOR ON
11	NC	12	DIRECTION SELECT
13	NC	14	STEP
15	0V	16	WRITE DATA
17	0V	18	WRITE GATE
19	0V	20	TRACK 00
21	NC	22	WRITE PROTECT
23	0V	24	READ DATA
25	0V	26	SIDE ONE SELECT

The FDD is equipped with a discrimination switch for the high density (HD) hole of an installed disk cartridge. Refer to item 8.3.14 as to the detailed explanation for density mode setting.
Refer to Table 1-1 and Table 1-2 as to operation mode and signal interface provided for this FDD.

2. DISK

(1) Work disk

90mm (3.5-inch) micro floppy disks which are mutually agreed between the customer and TEAC.

For 2MB mode : High density disk (2HD)

1MB mode : Normal density disk (2DD)

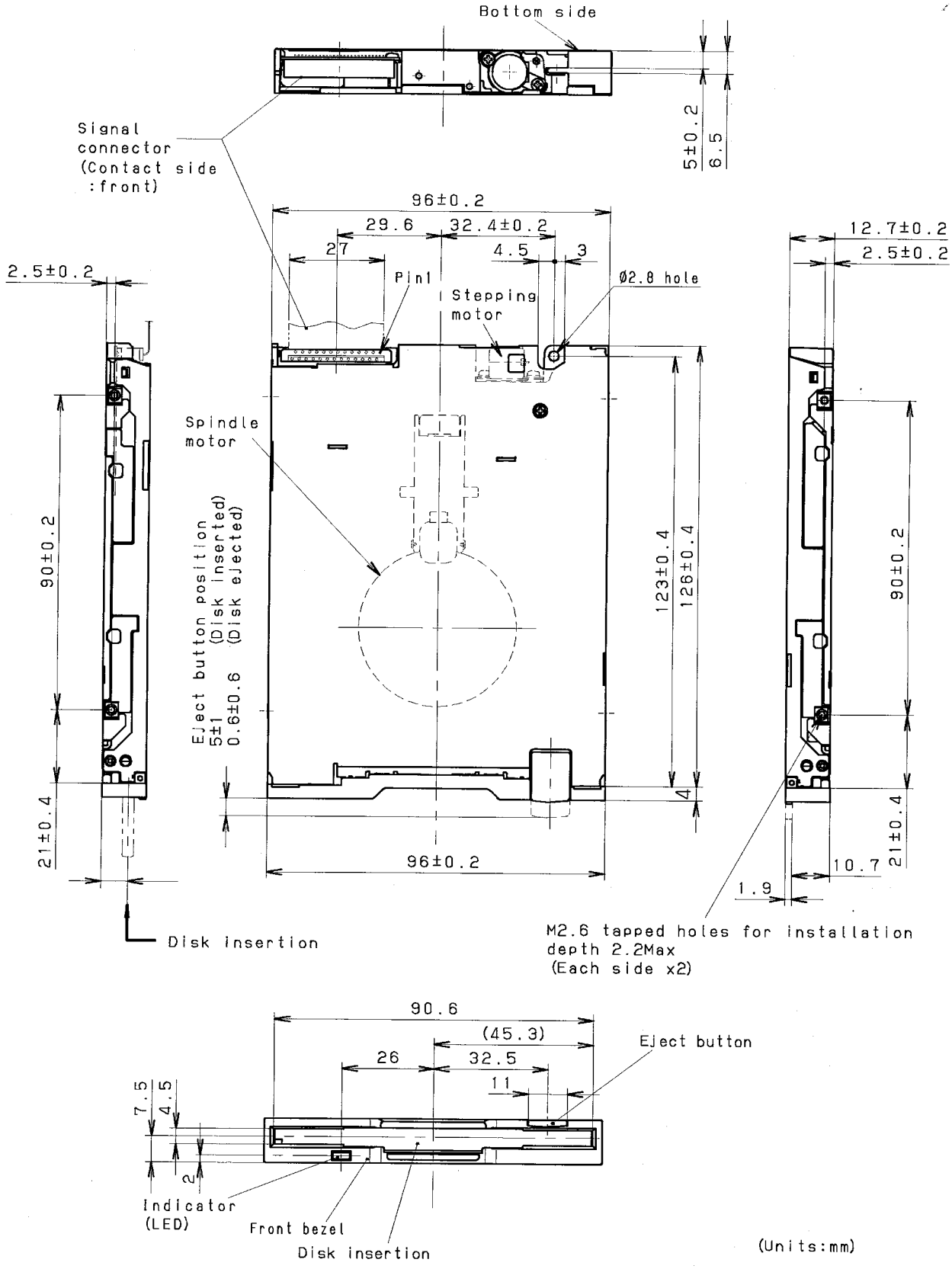
(2) Cleaning disk

The FDD does not require any cleaning disk. However, the dry type disk which is mutually agreed between the customer and TEAC is used when requiring a cleaning disk.

3. PHYSICAL SPECIFICATION

(Table 3-1) Physical specification

Width	96.0mm (3.78 in), Nom.
Height	12.7mm (0.50 in), Nom.
Depth	126mm (4.96 in), Nom., excluding front bezel
	130mm (5.12 in), Nom., including front bezel
Weight	157g (0.35 lbs), Nom., 162g (0.36 lbs), Max.
External view	See Fig. 3-1.
Cooling	Natural air cooling
Mounting	Mounting for the following directions are acceptable. (a) Front loading, mounted vertically. (b) Front loading, mounted horizontally with eject button right. (c) Mounting angle (a) and (b) should be less than 25° with front bezel up or down. Note : As to the other mounting directions than the above will be considered separately. Mounting directions of spindle motor up are prohibited.
Installation	With installation holes on the frame of the FDD. ϕ2.8 hole at the rear end can be also used for installation. Refer to Fig. 3-1.
Material of flame	Aluminium die-cast
Material of front bezel	PPHOX



(Fig. 3-1) FDD external view

4. OPERATIONAL CHARACTERISTICS

4.1 2MB Mode Data Capacity

(Table 4.1-1) 2MB mode data capacity

Recording method				FM	MFM
Data transfer rate			k bits/s	250	500
Tracks/disk				160	160
Innermost track bit density			bpmm (bpi)	343.19 (8,717)	686.38 (17,434)
Innermost track flux density			frpmm (frpi)	68.638 (17,434)	686.38 (17,434)
Data capacity	Unformatted		k bytes/track	6.25	12.5
			k bytes/disk	1,000	2,000
	Formatted	32 sectors/ track	k bytes/sector	0.128	0.256
			k bytes/track	4.096	8.192
			k bytes/disk	655.36	1,310.72
		18 sectors/ track	k bytes/sector	0.256	0.512
			k bytes/track	4.608	9.216
			k bytes/disk	737.28	1,474.56
		10 sectors/ track	k bytes/sector	0.512	1.024
			k bytes/track	5.12	10.24
			k bytes/disk	819.2	1,638.4

4.2 1MB Mode Data Capacity

(Table 4.2-1) 1MB mode data capacity

Recording method				FM	MFM
Data transfer rate			k bits/s	125	250
Tracks/disk				160	160
Innermost track bit density			bpmm (bpi)	171.61 (4,359)	343.19 (8,717)
Innermost track flux density			frpmm (frpi)	343.19 (8,717)	343.19 (8,717)
Data capacity	Unformatted		k bytes/track	3.125	6.25
			k bytes/disk	500	1,000
	Formatted	16 sectors/ track	k bytes/sector	0.128	0.256
			k bytes/track	2.048	4.096
			k bytes/disk	327.68	655.36
		9 sectors/ track	k bytes/sector	0.256	0.512
			k bytes/track	2.304	4.608
			k bytes/disk	368.64	737.28
		5 sectors/ track	k bytes/sector	0.512	1.024
			k bytes/track	2.56	5.12
			k bytes/disk	409.6	819.2

4.3 Disk Rotation Mechanism

(Table 4.3-1) Disk Rotation Mechanism

Spindle motor	DC brushless motor
Spindle speed	300rpm
Motor servo method	Frequency servo by ceramic oscillator
Motor/spindle connection	Motor shaft direct
Disk speed	The same as the spindle speed.
Long term speed variation (LSV)	±1.5% or less
Instantaneous speed variation (ISV)	±3% or less
Start time	480ms or less
Average latency	100ms
Ready waiting time	500ms or less for motor-on

4.4 Index Detection

(Table 4.4-1) Index Detection

Number of index	1per disk revolution
Detection method	Hall element
Detection cycle	200ms ±1.5%
Index burst detection timing error (with specified test disk)	±400μs or less

4.5 Track Construction

(Table 4.5-1) Track Construction

Track density	5.3 track/mm (135tpi)
	Track pitch 187.5μm
Number of cylinders	80 cylinders
number of tracks	160 tracks/disk
Outermost track radius (track 00)	Side 0 39.500mm (1.5551 in)
	Side 1 38.000mm (1.4961 in)
Innermost track radius (track 79)	Side 0 24.6875mm (0.9719 in)
	Side 1 23.1875mm (0.9129 in)
Positioning accuracy	±15μm or less, with specified test disk
	(Track 40, 23 ±2°C, 45 ~ 55%RH, horizontal)

4.6 Magnetic Head

(Table 4.6-1) Magnetic Head

Magnetic head	Read/write head with erase gap, 2 sets
Effective track width after trim erase	0.115 ±0.008mm (0.0045 ±0.0003 in)
Read/write gap azimuth error	0° ±18', with specified test disk

4.7 Track Seek Mechanism

(Table 4.7-1) Track Seek Mechanism

Head position mechanism	Stepping motor and lead screw
Stepping motor	4-phase, 20steps per revolution
Stepping motor drive	2 step per track
Track 00 detection method	Photo-interrupter
Track to track time	3ms (excludes setting time refer to item 8.3.4)
Setling time	15ms or less (excludes track to time)
Average track seek time	94ms (includes settling time)

4.8 Window Margin and Others

(Table 4.8-1) Window Margin and Others

Window Margin (with specified test disk, MFM method, PLL separator)		
	2MB mode	300ns or more
	1MB mode	600ns or more
Recommendable write pre-compensation		
	2MB mode	±125ns
	1MB mode	0 ~ ±125ns
Head load mechanism		Not equipped (The FDD becomes head load condition whenever a disk is installed.)
File protect mechanism		Detection of write inhibit hole by switch
Disk detection mechanism		Detection of disk installation by switch
Disk inserting force		6.86N (700g) or less at the center of disk
Disk ejecting force		11.76N (1200g) or less
Acoustic noise at 50cm		45dBA or less at 3ms seek operation
Disk type descriminating mechanism		Detection of HD hole by switch

5. ENVIRONMENTAL CONDITIONS

(Table 5-1) Environmental Condition

	Operating	Storage	Transportation
Ambient temperature	4 ~ 51.7°C (39 ~ 125°F)	-22 ~ 60°C (-8 ~ 140°F)	-40 ~ 65°C (-40 ~ 149°F)
Temperature gradient	20°C (36°F) or less per hour	30°C (54°F) or less per hour	30°C (54°F) or less per hour
Relative humidity	20 ~ 80% (no condensation) Max. wet bulb temperature shall be 29.4°C (85°F)	5 ~ 90% (no condensation) Max. wet bulb temperature shall be 40°C (104°F)	5 ~ 95% (no condensation) Max. wet bulb temperature shall be 45°C (113°F)
Vibraton	14.7m/s^2 (1.5G) or less (10 ~ 100Hz, 1 octave/min sweep rate)		19.6m/s^2 (2G) or less (10 ~ 100Hz, 1/4 octave/ min sweep rate)
	9.8m/s^2 (1.0G) or less (100 ~ 200Hz, 1 octave/ min sweep rate)		
	4.9m/s^2 (0.5G) or less (200 ~ 600Hz, 1 octave/ min sweep rate)		
Shock	Write & read: 49m/s^2 (5G)(11ms, 1/2 sine wave) or less		1,470m/s^2 (150G) (11ms, 1/2 sine wave) or less
	Read only: 98m/s^2 (10G) (11ms, 1/2 sine wave) or less		
Altitude	-300m (-980 feet) ~ 5,000m (16,400 feet)		

6. RELIABILITY

(Table 6-1) Reliability

MTTF		30,000 power on hours or more (for typical operation duty)
MTTR		When failure, the FDD should be replaced in unit of the drive and not repaired in unit of parts or assemblies.
Design component life		5 years
Disk life		3×10^6 passes/track or more
Disk insertion		1.5×10^4 times or more
Seek operation		1×10^7 random seeks or more
Preventive maintenance		Not required (for typical operation duty)
Error rate	Soft error	1 or less per 10^9 bits read A soft (recoverable) error is defined that it can be read correcty within three retries.
	Hard eror	1 or less per 10^{12} bits read A hard (unrecoverable) error is defined that cannot be read correstly within three retries. However, it is recommanded to be followed by a recalibration to track 00 and four additional retries.
	Seek error	1 or less per 10^6 seeks A seek error is defined that it can seek to target track within one retry including a recalibration to track 00.
Safety standard		Approved by UL, CSA and T Ü V
Electro-static discharge test		15kV (150pF, 330Ω) No hard error/or no component damage occur when the test is applied to the operator access area (front bezel area).

7. POWER INTERFACE

7.1 Required Power

The following specifications are applied at interface connector of the FDD.

(1) DC +12V : Not required

(2) DC +5V

(a) Voltage tolerance : ±10% (4.5 ~ 5.5V)

(b) Allowable ripple voltage : 100mVp-p or less (including spike noise)

(c) Current and power consumption

(Table 7.1-1) Current and power consumption

Operating mode		Average current		Average power	
		Typ.	Max.	Typ.	Max.
Stand-by		3.0mA	5.0mA	15mW	28mW
Read operation		0.17A	0.25A	0.85W	1.25W
Write operation		0.17A	0.25A	0.85W	1.25W
Seek operation	3ms	0.33A	0.4A	1.63W	2.2W
	6ms	0.39A	0.46A	1.95W	2.53W
Spindle motor start		0.37A	0.4A	1.85W	2.2W

Notes:

1. values of Typ. current and power are specified at 5.0V, while the values of Max. are at 5.5V (+10%) with a disk of large running torque.
2. Stand-by mode is defined at the stop condition of spindle motor and seek operation.
3. Rush current flows within 150ms after the motor start.
4. Short time peak current except for power-on surge is less than 0.6A.
5. Refer to item 9.4 as to the current consumption profile.

7.2 Power Interface Connector and Cable

(1) Power interface connector : Included in signal interface connector.
Refer to item 8.1 and Table 1-2.

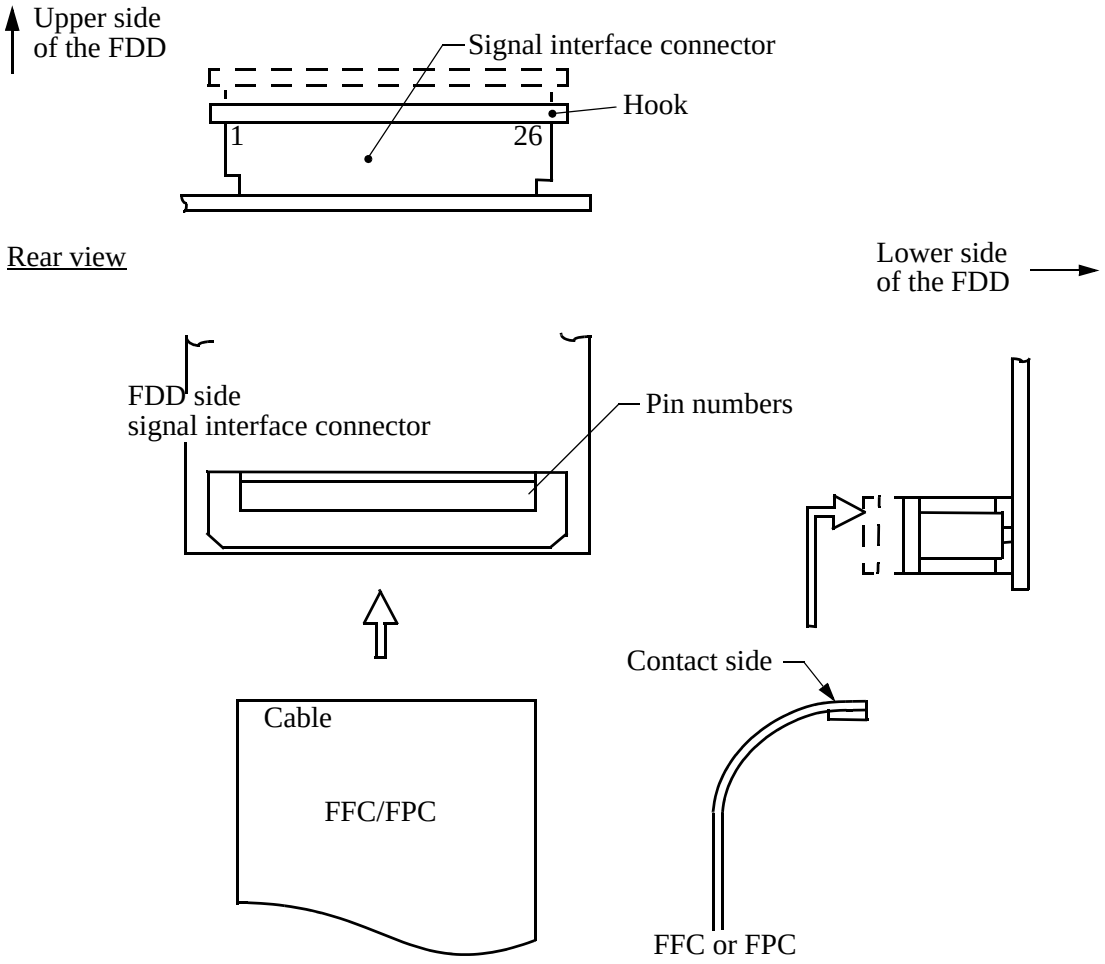
(2) Power interface cable : Included in signal interface cable.

8. SIGNAL INTERFACE

8.1 Signal Interface Connector and Cable

(Table 8.1-1) Signal Interface Connector and Cable

Signal interface connector	FDD side connector	SMK,P/N CFP 5126-0501 or SUMIKO-TEC, P/N LV1A026R000Z or Machrone, AF026N-A2E1T
	Pin numbers and pin pitch	1mm pitch, 26pin
	Connector external	See Fig. 8.1-1.
	Connector location	See Fig. 3-1.
Signal interface cable	Matched cable	1mm pitch, FFC or FPC, thickness 0.3mm, Sn plated
	Maximum cable length	50cm (1.65 feet)



Notes : 1. When disconnecting the cable, connector lock must be previously released by pulling up the hook.
2. When connecting the cable, fully insert the cable with the contact side being faced to the front side of the FDD, and then lock the connector by pushing down the hook.

(Fig. 8.1-1) Signal interface connector external view

8.2 Electrical Charactristics

"Vcc" means +5V power voltage supplied to the FDD.

8.2.1 FDD side receiver and driver

The specification in items (2) and (3) are applicable at the interface connector of the FDD.

(Table 8.2.1-1) FDD side receiver and driver

(1)	Circuit			See Fig. 8.2-2
(2)	Electrical characteristics of receiver	Input signals	Receiver	CMOS LSI
			LOW level (TRUE)	0 ~ 0.8V
			HIGH level (FALSE)	2V ~ Vcc
			LOW level input current	0.6mA, Max. (includes pull-up resistor current)
			HIGH level input current	2μA, Max.
		Pull-up resistor value		20kΩ ±50% Pull-up resistor is connected to each input signal line (unremovable)
(3)	Electrical characteristics of driver	Output signals	Driver	CMOS LSI (3-state output)
			LOW level (TRUE)	0 ~ 0.4V
			HIGH level (FALSE)	3.7V ~ Vcc
			LOW level output current	8mA, Max.
			HIGH level output current	-4mA, Max.
		High impedance state (not in DRIVE SELECTed condition) leakage current		±2μA, Max.

8.2.2 Host side receiver and driver

(Table 8.2.2-1) Host side receiver and driver

Receiver	CMOS, HCMOS, TTL, etc.
Driver	Compermentary or 3-state type CMOS/HCMOS, or totempole type TTL, etc.
Required sink current	FDD input current × Number of daisy-chained FDD

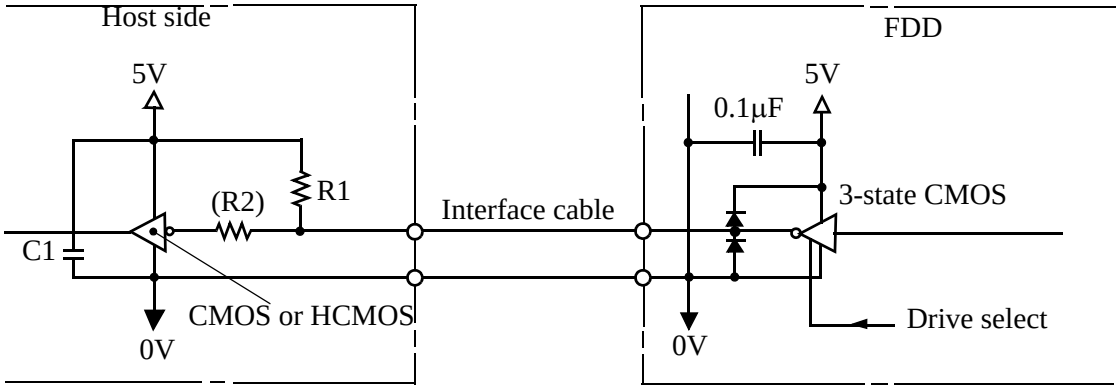
8.2.3 Recommended host side receiver circuit when CMOS or HCMOS is used

(1) Circuit example : Refer to Fig. 8.2-1.

(2) Pull-up resistor, R1 is for protecting the unstable input voltage during the high impedance state of the FDD output driver.
e.g. R1 value : 1 ~ 75kΩ

(3) Serial resistor, R2 may be for protecting the electrostatic destruction. It is not always required.
e.g. R2 value : 1 ~ 4.7kΩ[1]

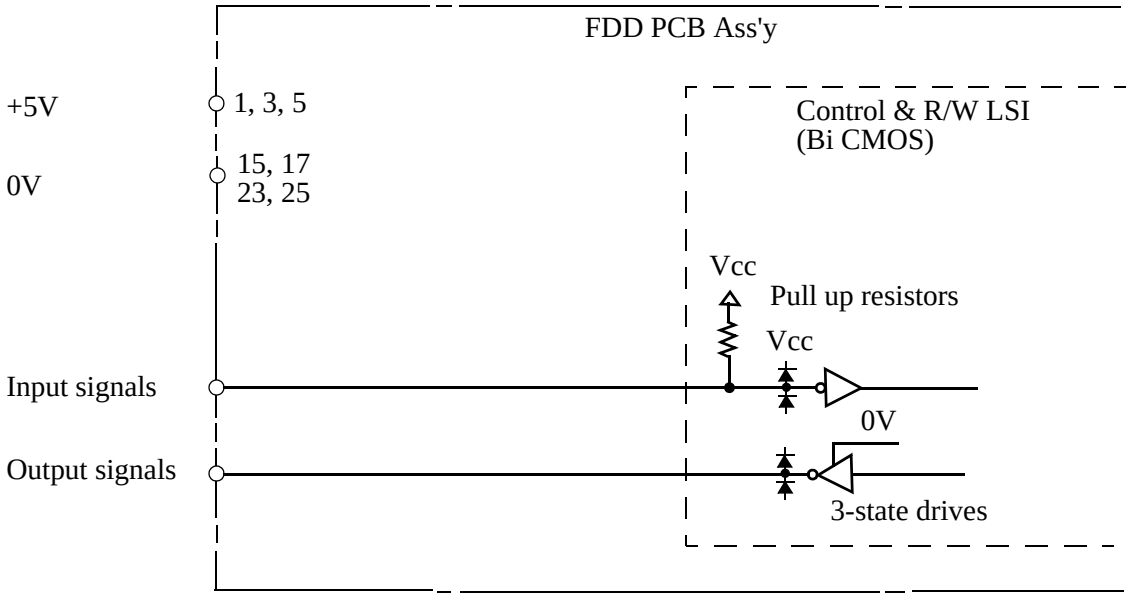
(4) Capacitor, C1 is for protecting the current shock when an HCMOS receiver is used. C1 should be mounted near the power pins of the receiver IC.
e.g. C1 value : 0.1μF, ceramic capacitor



(Fig. 8.2-1) A typical configuration of host side receiver

CAUTION: All the interface drivers and receivers of the FDD are equipped with protective diodes. Refer to Fig. 8.2-2.

1. When multiple FDDs are daisy-chained, applied power to the FDDs shall be the same source.
2. Applied power for the FDDs shall be the same as that for the host side interface circuits, if the protective resistor, R2 (more than 1kΩ) is not inserted.



(Fig. 8.2-2) FDD signal interface circuit

8.3 Input/Output Signals

In the following, input signals are those transmitted to the FDD while output signals are those transmitted from the FDD.

LOW level of the signals is TRUE unless otherwise specified.

Refer to Table 1-2 as to the signal needed in this specification.

8.3.1 DRIVE SELECT input signal

(1) Signal to select a specific FDD for operation in multiplex control.

(2) All the input/output signals except for the MOTOR ON is valid after this signal is made TRUE. The time required to be valid is 0.5μsec, Max. including transmission delay time of the DRIVE SELECT signal through the interface cable.

(3) Refer to item 11.1 as to the turn-on condition of the front indicator.

8.3.2 MOTOR ON input signal

(1) Level signal to rotate the spindle motor.

(2) The spindle motor reaches to the rated rotational speed within 480ms after this signal is made TRUE.

(3) Refer to item 11.2 as to the rotational condition of the spindle motor.

8.3.3 DIRECTION SELECT input signal

(1) Level signal to define the moving direction of the head when the STEP line is pulsed.

(2) Step-out (moving away from the center of the disk) is defined as HIGH level of this signal. Conversely, step-in (moving toward the center of the disk) is defined as LOW level of this signal.

(3) The signal shall maintain its level for 0.8μs, Min. prior to the trailing edge of the STEP pulse. Refer to Fig. 9.2-1.

8.3.4 STEP input signal

(1) Negative pulse signal to move the head. The pulse width shall be 0.8μs or more and the head moves one track space per one pulse.

(2) The access motion (head seek operation) is initiated at the trailing edge of the STEP pulse and completes within 18ms after starting the access including the settling time.

(3) For the subsequent motion in the same direction, the STEP pulses should be input with the interval of 3ms or more, while the pulses should be input with the interval of 4ms or more for a direction change. Refer to Fig. 9.2-1.
STEP pulses less than 3ms interval for the same direction or less than 4ms interval for a direction change may cause seek error.

(4) STEP pulses are ignored and the access motion is not initiated when one of the following conditions is satisfied.
(a) The WRITE PROTECT signal is FALSE and the WRITE GATE signal is TRUE.
(b) The TRACK 00 signal is TRUE and the DIRECTION SELECT signal is HIGH level (step-out).
(c) Step-in operation (DIRECTION SELECT signal is LOW level) from track 81.

(5) The STEP input signal is stored in the step counter inside the LSI without moving a head during unloading because an unload seek prohibition circuit is incorporated in the FDD.
Unloading conditions : 1. A disk is not installed.
2. The MOTOR ON signal is FALSE.
3. Within 200ms after the spindle motor starts rotating (through MOTOR ON).

(6) When the power-on recalibration is not terminated before unloading conditions are all released, it is executed after all the unloading conditions are released.

(7) When the valied STEP signal is input before unloading conditions are all released, the STEP commands stored are executed after all the unloading conditions are released.
(8) When the power-on recalibration is not terminated and valied STEP signal is input before unloading conditions are all released, the power-on recalibration and the STEP command are executed in this order after unloading conditions are all released.
(9) The STEP input signal is processed as before after all the unloading conditions are released and all the head moving commands are terminated.

8.3.5 WRITE GATE input signal

(1) Level signal to erase the written data and to enable the writing of new data.
(2) The FDD is set to write mode when the following logical expression is satisfied.
WRITE GATE * DRIVE SELECT * $\overline{\text{WRITE PROTECT}}$
(3) This signal shall be made TRUE after satisfying all of the following conditions.
(a) 18ms has been passed after the effective receival of the final STEP pulse.
(b) 100μs has been passed after the level change of the SIDE ONE SELECT signal.
(4) The following operations should not be done at least 650μs after this signal is changed to FALSE.
(a) Make the MOTOR ON signal FALSE.
(b) Start the head seek operation by the STEP pulse.
(c) Make the DRIVE SELECT signal FALSE.
(d) Change the level of the SIDE ONE SELECT signal.

8.3.6 WRITE DATA input signal

(1) Negative pulse signal to designate the contents of data to be written on a disk. The pulse width should be 0.2μs through 1.1μs and the leading edge of the pulse is used.
(2) WRITE DATA pulses are ignored while either of the following conditions is satisfied.
(a) The WRITE GATE signal is FALSE.
(b) The WRITE PROTECT signal is TRUE.
(3) This signal should be input according to the timing in Fig. 8.3-2.
It is recommended to stop the input of the WRITE DATA pulses during the read operation in order to avoid harmful cross talk.

8.3.7 SIDE ONE SELECT input signal

(1) Level signal to designate which side of a double sided disk is used for reading or writing.
(2) When this signal is HIGH level, the magnetic head on the side 0 surface (lower side) of the disk is selected, while the magnetic head on the side 1 surface (upper side) is selected when this signal is LOW level.
(3) The READ DATA pulse on a selected surface is valid more than 100μs after the change of this signal level.
(4) Write operation (the WRITE GATE signal is TRUE) on a selected surface shall be started more than 100μs after the change of this signal level.

8.3.8 TRACK 00 output signal

(1) Level signal to indicate the head is on track 00 (outermost track).
(2) This signal becomes valid in more than 2.8ms after the effective reception of the STEP pulse.
(3) This signal may be output on a different position from the actual head position because the signal is output through the step counter in the LSI during unloading.
(4) This signal is output on the actual position as before after all the unloading conditions are cleared.

8.3.9 INDEX output signal

(1) Negative pulse signal to indicate the start point of a track and one index pulse per one disk revolution is output.

(2) INDEX pulse is output when the following logical expression is satisfied.
Index detection * DRIVE SELECT * Ready state * Seek-complete

Notes : (a) Refer to item 8.3.13 as to the ready state.
(b) Seek-complete means the state that 15.8 ~ 17.9ms has been passed after the trailing edge of the final STEP pulse.

(3) Fig. 8.3-1 shows the timing of this signal. Leading edge of the pulse shall be used as the reference and pulse width is 1.5ms through 5ms.

8.3.10 READ DATA output signal

(1) Negative pulse signal for the read data from a disk composing clock bits and data bits together.

(2) Fig.6 shows the timing of this signal. Pulse width is 0.15μs through 0.8μs and the leading edge of the pulse shall be used as the reference.

(3) READ DATA pulse is output when the following logical expression is satisfied.
Read data detection * DRIVE SELECT * Write operation * Ready state * Seek-complete

Notes : (a) Refer to item 8.3.13 as to the ready state.
(b) Write operation is the state while the WRITE GATE input signal is FALSE and erase delay time has been passed after the WRITE GATE signal changed to FALSE.
(c) Refer to item 8.3.9 (2) as to the seek-complete.

(4) Output pulse is valid while all of the following conditions are satisfied.
(a) 18ms has been passed after the effective receival of the final STEP pulse.
(b) 100μs has been passed after the level change of the SIDE ONE SELECT signal.
(c) 650μs (2MB mode) or 690μs (1MB mode) has been passed after the WRITE GATE signal is changed to FALSE.

8.3.11 WRITE PROTECT output signal

(1) Level signal to indicate that the write inhibit hole of an installed disk is open.

(2) When this signal is TRUE, data on the disk are protected from miserasing and write operation is inhibited.

8.3.12 DISK CHANGE output signal

(1) Level signal to indicate that a disk in the FDD is ejected.

(2) This signal changes to TRUE when either of the following conditions is satisfied.
(a) Power on.
(b) A disk is removed.

(3) The signal returns to FALSE when both of the following conditions are satisfied. Refer to Fig. 8.3-4
(a) A disk has been installed.
(b) A STEP command is received when the DRIVE SELECT signal is TRUE.

8.3.13 READY output signal

(1) Level signal to indicate that the FDD is in ready state for read and write operations.

(2) The FDD goes to ready state when all of the following conditions are satisfied.
(a) The FDD is powered on.
(b) A disk is installed.
(c) A motor-on command is TRUE and 480ms, approx. has been passed.
(d) An INDEX pulse has been detected after motor-on command.

(3) Required time for this signal to be TRUE after the start of the spindle motor is 500ms or less.
(4) When a motor-on command is made FALSE, this signal is also changed to FALSE within 0.3ms.

8.3.14 Output signals for density mode setting (HD OUT)

Every FDD model, there are any basic methods for setting the density mode of the FDD as shown in the following.
Use the applicable method for the FDD in contents shown below.

8.3.14.1 Method for switchable of density mode between HIGH DENSITY and NORMAL DENSITY

(1) Method A without using any interface signal (OPEN)
  (a) Interface signal is not used between the FDD and host-controller.
    Density mode of the FDD and host system are determined independently.
  (b) Density mode of the FDD is automatically set by discriminating the HD hole of an installed disk. If the density mode of the FDD is not coincident with that of the host controller, data errors always occur at read operation.
(2) Methord B using HD OUT output signal
  (a) Density mode of the FDD is automatically set by discriminating the HD hole of an installed disk.
  (b) HIGH or LOW level of the HD OUT signal from the FDD is used to inform host controller which type of disk is installed in the FDD. And the density mode of the host is automatically determined according to this signal.
  (c) Table 8.3.14.1-1 shows the meaning of the logic level.

(Table 8.3.14.1-1) Meaning of the logic level

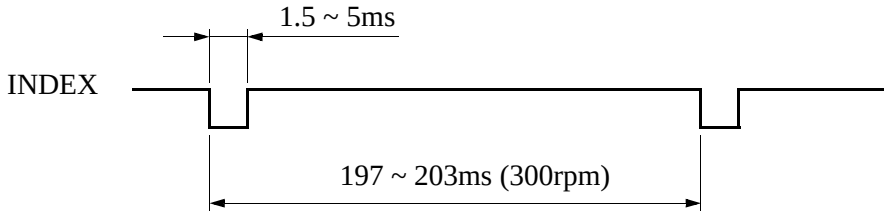
Signal name	Logic level	HIGH LEVEL at HIGH DENDITY
HD OUT	HIGH	2HD disk or no disk
	LOW	2DD disk

8.3.15 NO CONNECTION (NC)

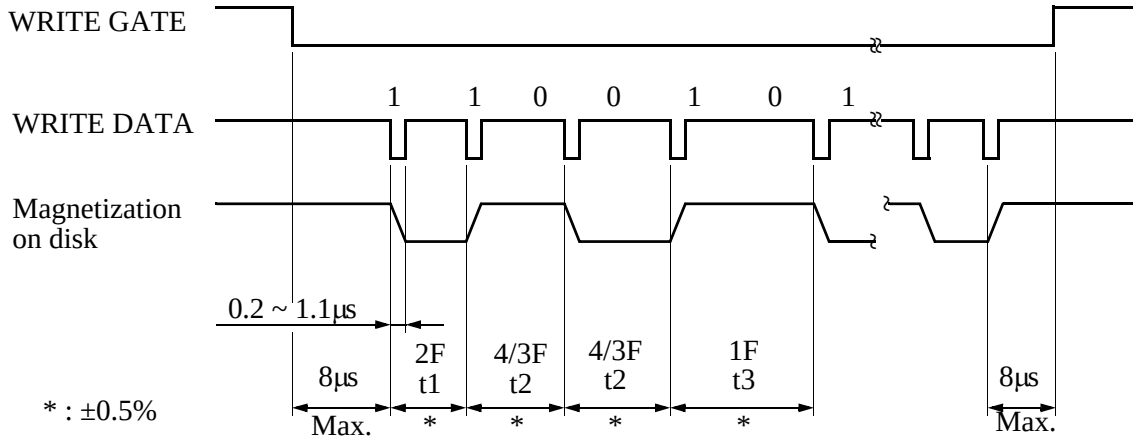
The NC pins are electrically isolated from any other circuit in the FDD.

8.3.16 Treatment of not-used signals

If some of the provided input/output signals are not necessary for your application, keep the unused signal lines open or pull up by an appropriate resistor value (refer to item 8.2.2) at the host side.

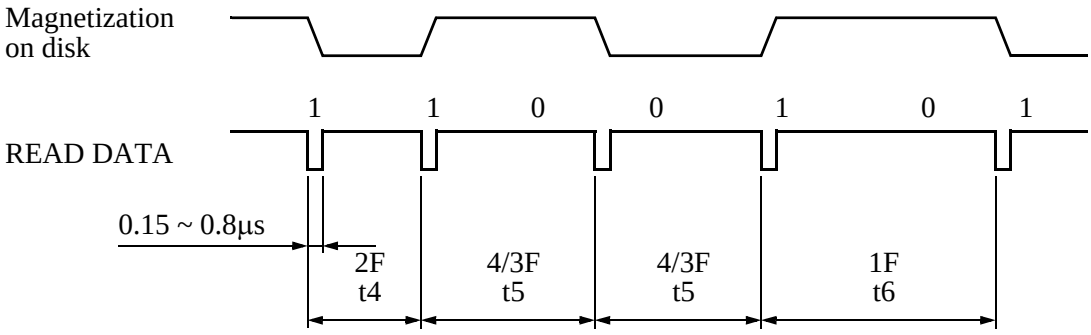


(Fig. 8.3-1) INDEX timing



Density mode	rpm	t1	t2	t3
2MB mode	300	2µs, Nom.	3µs, Nom.	4µs, Nom.
1MB mode	300	4µs, Nom.	6µs, Nom.	8µs, Nom.

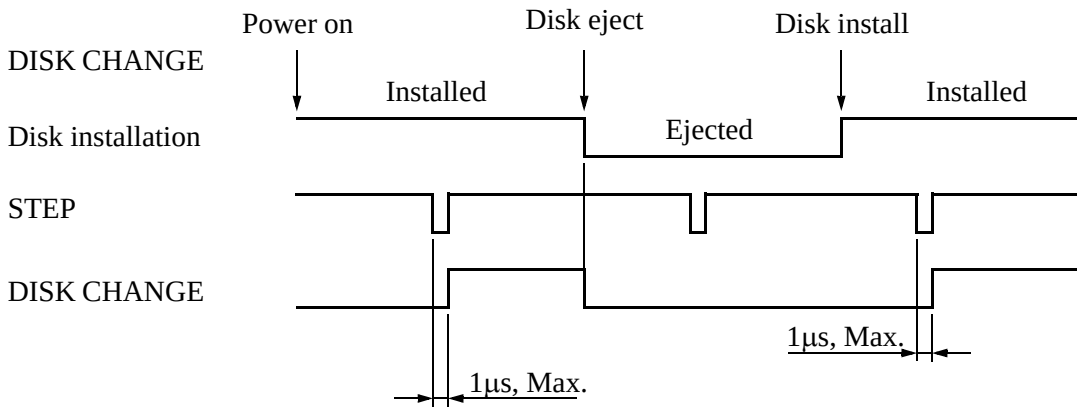
(Fig. 8.3-2) WRITE DATA timing (MFM method)



Note : READ DATA pulse will be detected within t7 from is nominal position. (When PLL separator is used with recommended write pre-compensation.)

Density mode	rpm	t4	t5	t6	t7
2MB mode	300	2µs, Nom.	3µs, Nom.	4µs, Nom.	±350ns
1MB mode	300	4µs, Nom.	6µs, Nom.	8µs, Nom.	±700ns

(Fig. 8.3-3) READ DATA timing (MFM method)



Note : To simplify the timing chart, the DRIVE SELECT signal is assumed always TRUE in the above figure.

(Fig. 8.3-4) DISK CHANGE signal timing

9. CONTROL SEQUENCE

9.1 Power-on

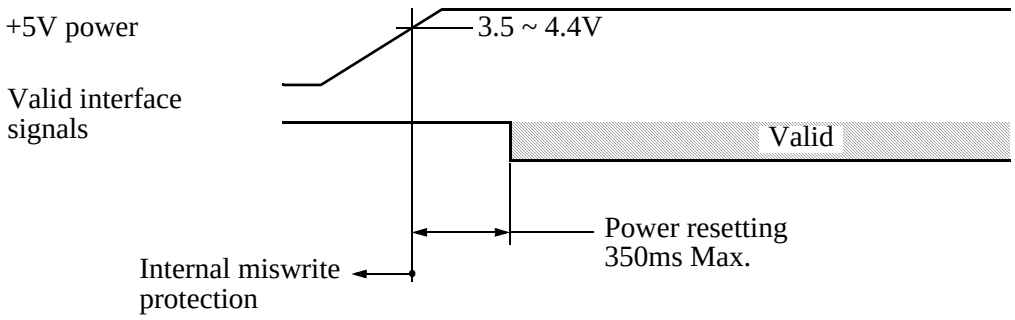
(1) Protection against power on and off

(a) In the transient period when the +5V power is lower than 3.5V, the FDD is protected against miswriting and miserasing whatever the state of input signals are.

(b) Except for the condition of item (a), the FDD is protected against miswriting and miserasing as long as the WRITE GATE input signal does not change to TRUE.

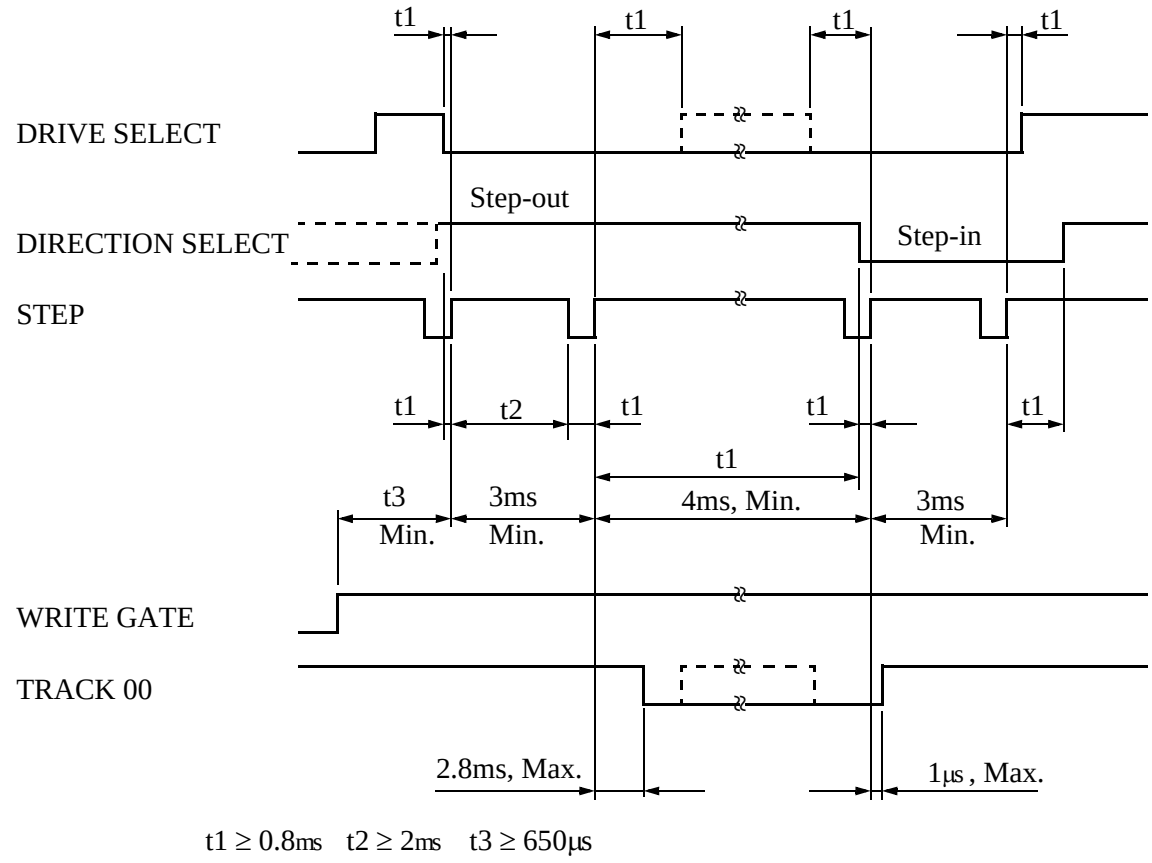
(2) Power reset time in FDD.

Less than 350μs, including the initial reset of the FDD.



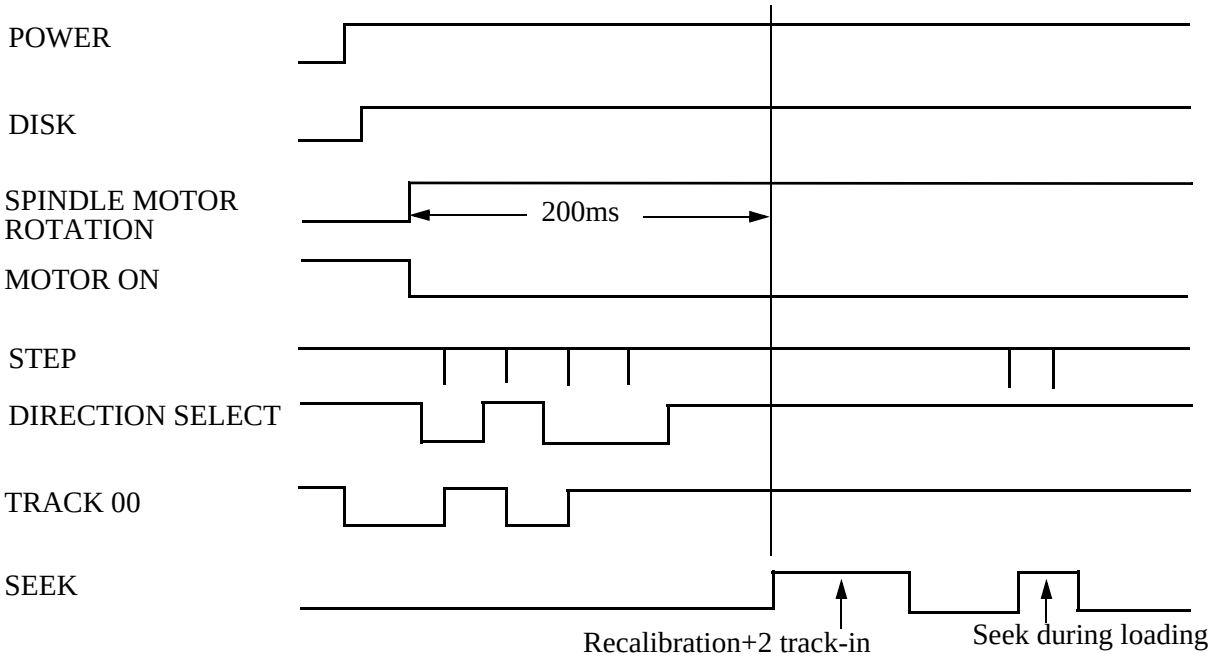
(Fig. 9.1-1) Power on sequence

9.2 Seek Operation



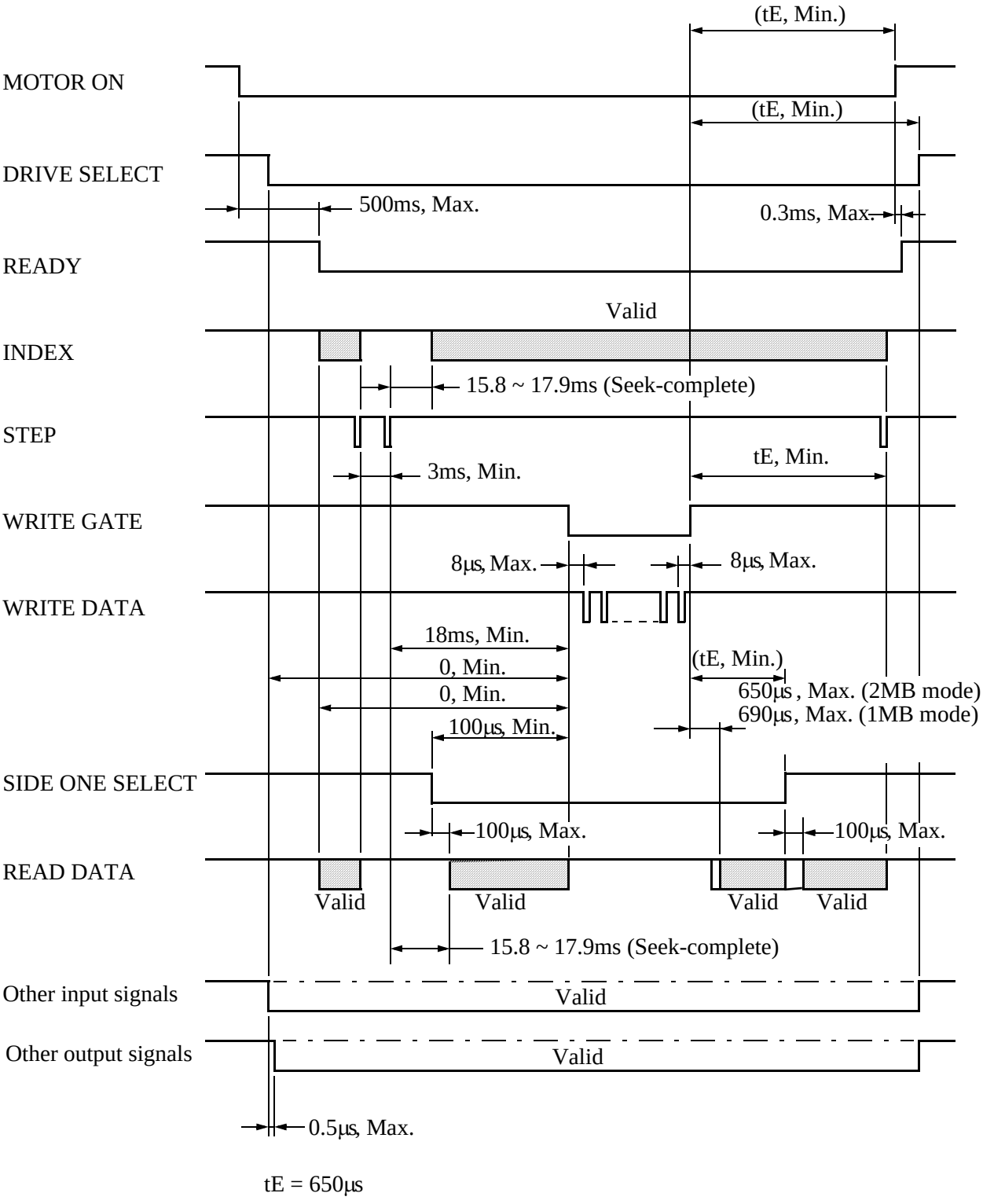
t1 ≥ 0.8ms t2 ≥ 2ms t3 ≥ 650μs

(Fig. 9.2-1) Seek operation timing



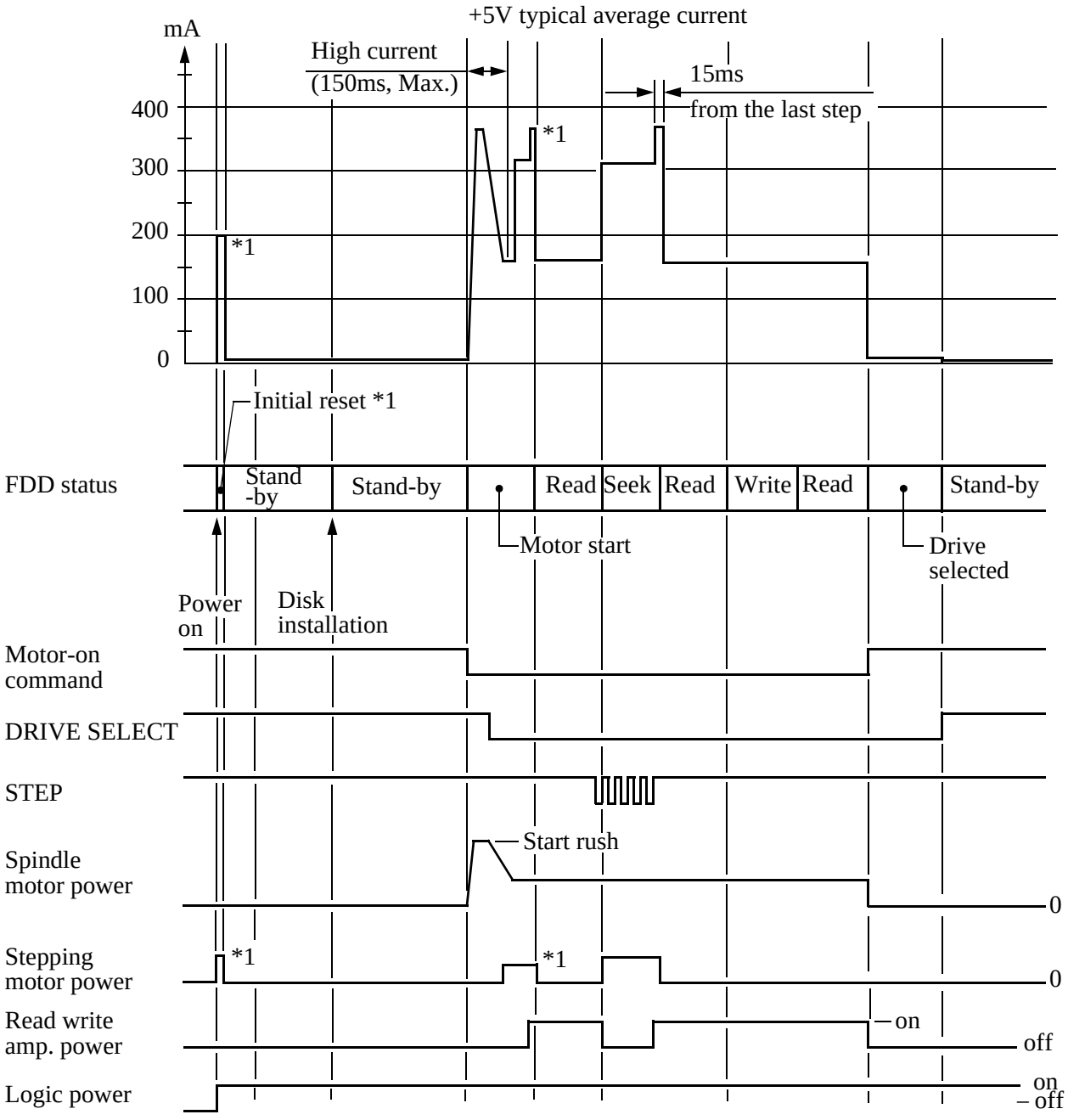
(Fig. 9.2-2) Timing during unloading

9.3 Read Write Operation



(Fig. 9.3-1) Read/Write operation timing

9.4 Current Consumption Profile



*1 Changed

(Fig. 9.4-1) Current profile of new drive

(1) Stand-by mode

When both of the following conditions are satisfied, FDD goes to the stand-by mode (low power consumption mode).

(a) The spindle motor stops.

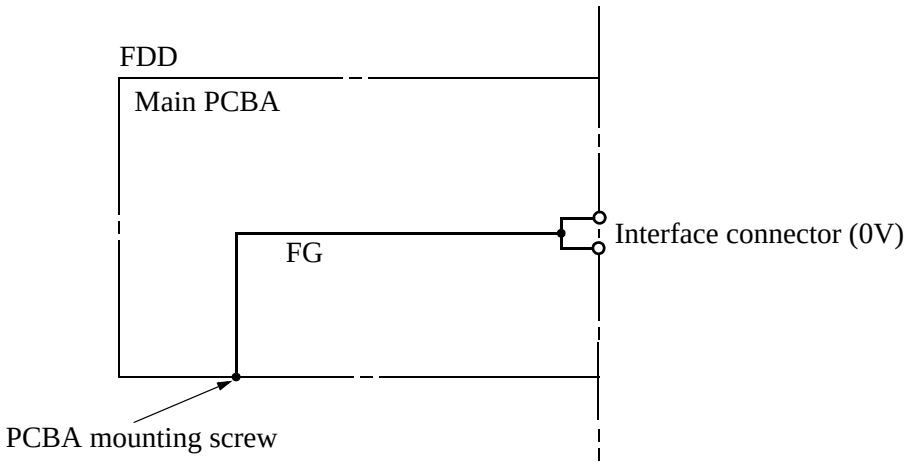
(b) Not in the seek operation (including the settling time).

Note : In the stand-by mode, the FDD can immediately respond to a command from host controller with no restriction.

If the polling operation of the DRIVE SELECT line is done in the stand-by mode, current flows intermittently and +5V current slightly increases.

10. FRAME GROUNDING

The FDD frame is electrically connected to DC 0V by the mounting screw of the main PCBA. (See Fig. 10-1).



(Fig. 10-1) Frame ground internal connection

11. TURN ON CONDITION OF INDICATOR AND SPINDLE MOTOR

11.1 Front Indicator

The indicator (LED) turns on while the DRIVE SELECT signal is TRUE and the FDD is in ready state. Refer to item 8.3.13 as to the ready state.

11.2 Spindle Motor

The spindle motor rotates while the MOTOR ON signal is TRUE. While no disk is installed, the spindle motor does not rotate at any condition.